Circuit-Level Considerations for an Ultra-Low Voltage FPGA with Unidirectional, Single-Driver Routing Fabric

Peter Grossmann, Miriam Leeser
26 September 2011

The Lincoln Laboratory portion of this work was sponsored by the United States Government under Air Force contract number FA8721-05-C-0002. The opinions, interpretations, conclusions and recommendations are those of the authors and are not necessarily endorsed by the United States Government.
Subthreshold FPGA Motivation

• Low power systems benefit from FPGAs
  – Improved energy efficiency/performance vs. microcontroller
  – Improved design via reconfigurability
  – Lower cost vs. ASIC

• State of the art low power FPGAs: 10s to 100s of mW

• Ultra-low power applications require 10s to 100s of $\mu$W
  – Wireless sensor networks
  – RFID
  – Digital hearing aids

• Ultra-low power budgets motivate extreme voltage scaling
  – Subthreshold supply voltages yield peak energy efficiency
FPGA Architecture Overview

- Array of tiles
  - Configurable Logic Blocks (CLBs)
  - Programmable Routing Channels

- Tile periphery connects to I/O blocks

- Logic functions, routing connectivity programmed via SRAM

A. Sharma, “Place and Route Techniques for FPGA Architecture Advancement,” University of Washington, 2005.
FPGA Tile Architecture Used In This Work

- Cluster-based island style tile
- 8-BLE clusters – good cluster count for low-power FPGAs
- Logically equivalent inputs -- improves routing flexibility
- Directional, single driver routing

![Diagram of FPGA Tile Architecture](image)
Three Sub-Vt FPGA Circuit Design Decisions

- Configuration bit storage
- Two-input multiplexer design choices
- Wide-input multiplexer design choices

Goal: Minimize Power, Delay, and Area
- Static power especially critical
- Sacrificing delay for static power acceptable
- Sacrificing area for power might be acceptable
  - Area no longer critical for delay reduction
  - Logic capacity requirements for many ultra-low power applications are modest
  - Reducing die size for yield, cost considerations may drive area requirements
**Standard 6T SRAM Bit Cell**

- Subthreshold FPGA SRAM use case: slow writes, no reads
- Cross-coupled inverters directly drive configuration inputs
- Primary goals: low area, low static power

**6T Latch**
Leaf Cell Implementation—Multiplexer

Key Considerations

- **Process technology matters**
  - IBM 0.18µm SOI

- **Input type matters**
  - Fast select lines needed for LUT
  - Fast non-select lines needed for routing muxes

- **Static power matters**
  - Many mux instances will be unused logic, routing resources

- **Area still matters**
  - Each tile will contain the equivalent of ~1300 2-input muxes
Multiplexer Style Comparison

- Significant area, delay penalties for improved power in DTMOS
- Transmission gate multiplexer power not acceptable
- If area matters, plain old static CMOS appears to be best choice

<table>
<thead>
<tr>
<th></th>
<th>nmux2</th>
<th>nmuxs2</th>
<th>nmux_dtmos2</th>
<th>tnmux2</th>
<th>tnmux_dtmos2</th>
<th>nmux_sbc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Avg. Current</td>
<td>1.00</td>
<td>0.98</td>
<td>0.45</td>
<td>2.32</td>
<td>0.75</td>
<td>0.72</td>
</tr>
<tr>
<td>Avg. Static Current</td>
<td>1.00</td>
<td>1.07</td>
<td>0.32</td>
<td>2.31</td>
<td>0.66</td>
<td>0.73</td>
</tr>
<tr>
<td>A/B-Y Delay</td>
<td>1.00</td>
<td>0.95</td>
<td>1.40</td>
<td>0.86</td>
<td>1.18</td>
<td>6.65</td>
</tr>
<tr>
<td>S-Y Delay</td>
<td>1.00</td>
<td>1.20</td>
<td>1.28</td>
<td>0.66</td>
<td>1.09</td>
<td>7.13</td>
</tr>
<tr>
<td>Area</td>
<td>1.00</td>
<td>1.00</td>
<td>2.60</td>
<td>0.99</td>
<td>2.59</td>
<td>2.30</td>
</tr>
</tbody>
</table>
Wide Input Multiplexer Power Gating

- State-based power gating
- No additional programming bits required
- Practical for FPGAs—wakeup time is irrelevant for routing muxes

Possible Approaches
- “Full” – power gate all muxes not on the selected path; requires additional logic
- “Flat” – larger loads on sleep transistors
- “Hierarchical” – reduces input capacitance on final select bit, lighter loads on sleep transistors
## Comparison of State-Based Power Gating Implementations

<table>
<thead>
<tr>
<th></th>
<th>16:1 LF Mux</th>
<th>16:1 LF Mux, Full</th>
<th>16:1 LF Mux, Hierarchical</th>
<th>16:1 LF Mux, Flat</th>
</tr>
</thead>
<tbody>
<tr>
<td>Avg. Delay (ns)</td>
<td>1.00</td>
<td>2.01</td>
<td>1.64</td>
<td>1.36</td>
</tr>
<tr>
<td>Avg. Static Current (nA)</td>
<td>1.00</td>
<td>1.28</td>
<td>0.57</td>
<td>0.56</td>
</tr>
<tr>
<td>Area (µm²)</td>
<td>1.00</td>
<td>2.91</td>
<td>1.76</td>
<td>1.60</td>
</tr>
</tbody>
</table>

- Full approach requires too much logic
- Flat, hierarchical approaches show good efficiency (8/15 = 0.53)
- Most hierarchical, flat area overhead due to isolation of power rails
Conclusion

• Use of 6T latch eliminates need to design around subthreshold SRAM noise margins for configuration bits

• Multiple area/delay/power tradeoffs available for two-input multiplexers to implement routing fabrics

• State-based power gating for wide input multiplexers consume ≈ (N/2)/(N-1) times the static power of non-power gated counterparts

• Subthreshold FPGAs benefit from circuit design that is aware of FPGA use cases
Thank You

- MIT Lincoln Laboratory
  - Lincoln Scholars Program
  - Group 83
  - Group 88
  - LLCAD

- PhD Committee
  - Miriam Leeser (Advisor)
  - Nicol McGruer (Northeastern)
  - Anantha Chandrakasan (MIT)
  - Peter Wyatt (MITLL)
Benefits of Unidirectional Routing Fabric

- Simplified circuitry for drivers – no tristate buffers required
- Reduced capacitance on routing wires due to shorter wires and smaller loads
- Net improvement in area-delay product
- Doubling wire count vs. bidirectional routing resources not necessary


Lemieux et. al (2004)