Miriam E. Leeser

Dept. of Electrical and Computer Engineering
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Education

Ph.D. in Computer Science, February 1988
Computer Laboratory, Cambridge University. Supported by Acorn Computers, Ltd.
Thesis: *Reasoning about the Function and Timing of Integrated Circuits with Prolog and Temporal Logic*. Supervisor: W. F. Clocksin

Diploma in Computer Science, August 1984
Computer Laboratory, Cambridge University, Cambridge England
Project: *A Flavors Package for Cambridge Lisp*. Supervisor: B. K. Boguraev

Bachelor of Science with distinction, May 1980
School of Electrical Engineering, Cornell University, Ithaca, NY

Primary Employment

Professor (July 2006 - present)
Northeastern University, Dept of Electrical and Computer Engineering

Interim Chair (August 2016 - December 2017)
Northeastern University, Dept of Electrical and Computer Engineering

Associate Professor (January 1996 - June 2006)
Northeastern University, Dept of Electrical and Computer Engineering

Associate Professor (July, 1995 - June 1996)
Assistant Professor (July, 1988 - June 1995)
Cornell University, School of Electrical Engineering

Summary of Achievements

• NSF Young Investigator Award, 1992.
• Continuously funded since 1990. Funding sources include DOD, NSF, NASA, NRO, and several companies including Intel, Mathworks, Mercury Computer Systems and Xilinx Corporation.
• 18 PhD students graduated. 30 MS students graduated with thesis. 7 students in progress.
• Over 180 refereed publications, including 35 journal articles published or accepted. h index 29.
• Associate Editor, ACM Transactions on Reconfigurable Systems, EURASIP Journal on Embedded Systems, International Journal of Reconfigurable Computing.
• Senior Member: ACM, IEEE, Society of Women Engineers.
• Best paper awards at High Performance Embedded Computing, Symposium on Application Accelerators for High Performance Computing.
• 1 US Patent Awarded.

Secondary Apppointments

Visiting Researcher (September 2010 - June 2011)
Robot Locomotion Laboratory, Mass. Inst. of Technology

JEOM Visiting Faculty Fellowship(May 2008 - August 2008)
Air Force Research Laboratory, Rome NY

Honorary Research Fellow (January 2003 - July 2003)
Auckland University, Dept of Electronic and Electrical Engineering

Visiting Scientist (June, 2002 - December 2002)
MIT Lincoln Laboratories, Lexington MA

Patent

US PATENT 4967344: INTERCONNECTION NETWORK FOR MULTIPLE PROCESSORS, Inventors: D. Scavezze, M. Leeser, G. Kammerer, and W. Prescott. Assigned to Codex Corporation, Mansfield MA. October 30, 1990.

Honors and Awards

Best paper award, Symposium on Application Accelerators in High-Performance Computing, 2011.
Best paper award, High Performance Embedded Computing Conference, 2007.
National Science Foundation National Young Investigator Award, 1992–97.
Acorn Computers Ltd Scholarship 1984–87.
Overseas Research Student Award 1984–87.

Editorships, Memberships and Advisory Boards

Associate Editor ACM Transactions on Reconfigurable Systems.
Associate Editor EURASIP Journal on Embedded Systems.
Associate Editor International Journal of Reconfigurable Computing.
Member PeerJ Computer Science Academic Editorial Board.
Senior Member IEEE, **Senior Member** Society of Women Engineers.
Senior Member Association for Computing Machinery (ACM).
Member President's Council of Cornell Women (PCCW)
Member Mathworks Advisory Board

Guest Editor
ACM Transactions on Reconfigurable Technology and Systems: Special issue on best papers from FCCM 2013. Eurasip Journal on Embedded Systems Special Issue on FPGA Supercomputing Platforms, Architectures and Techniques for Accelerating Computationally Complex Algorithms. January 2009.
Journal of Parallel and Distributed Computing Special Issue on General-Purpose Processing Using Graphics Processing Units. Oct. 2008.
Eurasip Journal on Embedded Systems Special Issue on Field-Programmable Gate Arrays in Embedded Systems, 2006.

Publications

Book

Hardware Specification, Verification, and Synthesis: Mathematical Aspects, Miriam Leeser and Geoffrey Brown, eds. Springer-Verlag Lecture Notes in Computer Science No. 408, January 1990.

Refereed Journal Articles

35. "Hardware-Software Codesign of Wireless Transceivers on Zynq Heterogeneous Systems," B. Drozdenko, M. Zimmermann, T. Dao, K. Chowdhury, and M. Leeser. *IEEE Transactions on Emerging Topics in Computing*, Special Issue on Next Generation Wireless Computing Systems. DOI: https://doi.org/10.1109/TETC.2017.2651054. To appear.

34. "Open Source Variable Precision Floating Point Library for Major Commercial FPGAs," Xin Fang and Miriam Leeser. *ACM Transactions on Reconfigurable Technology and Systems.* vol. 9, no. 3, July 2016. DOI: http://dx.doi.org/10.1145/2851507.

33. "High-Level System Design of IEEE 802.11b Standard-Compliant Link Layer for MATLAB-based SDR," R. Subramanian, B. Drozdenko, E. Doyle, R. Ahmed, M. Leeser, and K. R. Chowdhury, *IEEE Access*, vol. 4, pp. 1494 - 1509, 2016. DOI: 10.1109/ACCESS.2016.2553671.

32. "Validity and Reliability of Kinect Skeleton for Measuring Shoulder Joint Angles," Meghan Huber, Amee L. Seitz, Miriam Leeser and Dagmar Sternad. *Physiotherapy.* Vol. 101, No. 4, pp. 389-393. December, 2015. DOI: http://dx.doi.org/10.1016/j.physio.2015.02.002.

31. "Kernel Specialization Provides Adaptable GPU Code for Particle Image Velocimetry," N. Moore, M. Leeser and L. Smith King. *IEEE Trans. on Parallel and Distributed Systems.* vol. 26, no. 4, pp. 1049-1058, April 2015. DOI: 10.1109/TPDS.2014.2317721.

30. "Fast reconstruction of 3D volumes from 2D CT projection data with GPUs," Miriam Leeser, Saoni Mukherjee and James Brock. *Biomed Central Research Notes 2014, 7:582.* DOI:10.1186/1756-0500-7-582.

29. "Minimum Energy Analysis and Experimental Verification of a Latch-Based Subthreshold FPGA," P. J. Grossmann, M. E. Leeser, and M. Onabajo, *IEEE Trans. on Circuits and Systems II: Express Briefs* Vol. 59, no. 12, pp. 942–946, Dec. 2012. DOI: https://doi.org/10.1109/TCSII.2012.

28. "The effect of temporal impulse response on experimental reduction of photon scatter in time-resolved diffuse optical tomography," Niksa Valim, James Brock, Miriam Leeser and Mark Niedre. *Physics in Medicine and Biology.* Vol. 58, No. 2, pp. 335-349, Dec. 2012.

27. "VForce: An Environment for Portable Applications on High Performance Systems with Accelerators," Nicholas Moore, Miriam Leeser and Laurie Smith King. *Journal of Parallel and Distributed Computing,* Elsevier. Special issue on Accelerators for High Performance Computing. Vol. 72, No. 9, pp. 1144-1156, Sept. 2012.

26. "The Challenges of Writing Portable, Correct and High Performance Libraries for GPUs," Miriam Leeser, Devon Yablonski, Dana Brooks, Laurie Smith King. *ACM SIGARCH Computer Architecture News.* Volume 39 Issue 4, pages 2-7, Sept. 2011.

25. "VFloat: A Variable Precision Fixed- and Floating-Point Library for Reconfigurable Hardware," Xiaojun Wang and Miriam Leeser. *ACM Transactions on Reconfigurable Technology and Systems*. Vol. 3 No. 3, September 2010.

24. "A Truly Two Dimensional Systolic Array FPGA Implementation of QR Decomposition," Xiaojun Wang and Miriam Leeser. *ACM Transactions on Embedded Computer Systems*. Vol. 9 No. 1, October 2009.

23. "Parallel Backprojection: A Case Study in High-Performance Reconfigurable Computing," Ben Cordes and Miriam Leeser. *EURASIP Journal on Embedded Systems Special Issue on FPGA Supercomputing Platforms, Architectures and Techniques for Accelerating Computationally Complex Algorithms*. Volume 2009.

22. "Efficient Communication Between the Embedded Processor and the Reconfigurable Logic on an FPGA," Joshua Noseworthy and Miriam Leeser. *IEEE Transactions on VLSI Systems*, Vol. 16 No. 8, pp. 1083–1090, Aug. 2008.

21. "Dynamo: A Runtime Partitioning System for FPGA-based HW/SW Image Processing Systems," Heather Quinn, Miriam Leeser and Laurie Smith King. *Journal of Real-Time Image Processing*, Vol. 2 No. 4, pp. 179–190, Dec. 2007.

20. "Vforce: An Extensible Framework for Reconfigurable Supercomputing," Nicholas Moore, Albert Conti, Miriam Leeser and Laurie Smith King. *Computer*. Published by the IEEE, pp. 39– 49, March, 2007.

19. "Real-Time Particle Image Velocimetry for Feedback Loops Using FPGA Implementation," Haiqian Yu, Miriam Leeser, Gilead Tadmor and Stefan Siegel. *Journal of Aerospace Computing, Information, and Communication*. Vol. 3 Issue 2, pp. 52–62, Feb. 2006.

18. "Enabling MPEG-2 Video Playback in Embedded Systems Through Improved Data Cache Efficiency," Peter Soderquist, Miriam Leeser and Juan Carlos Rojas. *IEEE Transactions on Multimedia*. Vol. 8, No. 1, pp. 81–89, Feb. 2006.

17. "Parallel-Beam Backprojection: An FPGA Implementation Optimized for Medical Imaging," Miriam Leeser, Srdjan Coric, Eric Miller, Haiqian Yu and Marc Trepanier. *Journal of VLSI Signal Processing*. Vol. 39 No. 3, pp. 295–311, 2005.

16. "Accurate Power Estimation for Sequential CMOS Circuits using Graph-based Methods," Miriam Leeser and Valerie Ohm. *VLSI Design, An International Journal of Custom-Chip Design, Simulation and Testing*. Special Issue on Low-Power Design. Vol. 12 No. 2, pp. 187–203, 2001.

15. "Design and Analysis of a Dynamically Reconfigurable Three-Dimensional FPGA," Silviu Chiricescu, Miriam Leeser and M. Michael Vai. *IEEE Transactions on VLSI Systems*, Special Issue on Reconfigurable and Adaptive VLSI Systems. Vol. 9 No. 1, pp. 186–196, February 2001.

14. "A Data-Centric Approach to High-Level Synthesis," Shantanu Tarafdar and Miriam Leeser. *IEEE Transactions on Computer-Aided Design*, Vol. 19 No. 11, pp. 1251–1267, November 2000.

13. "HML: A Novel Hardware Description Language, and its Translation t o VHDL," Yanbing Li and Miriam Leeser. *IEEE Transactions on VLSI Systems*, pp. 1–8, January 2000.

12. "Rothko: A Three Dimensional FPGA," M. Leeser, W. Meleis, M. Vai, S. Chiricescu, W. Xu and P. Zavracky. *IEEE Design and Test of Computers*, Vol. 15 No. 1, pp. 16–23, January–March, 1998.

11. "Division and Square Root: Choosing the Right Implementation," Peter Soderquist and Miriam Leeser. *IEEE Micro*, Vol. 17 No. 4, pp. 56–66, July/August 1997.

10. "Area and Performance Tradeoffs in Floating-Point Division and Square Root Implementations," Peter Soderquist and Miriam Leeser. *ACM Computing Surveys*, Vol. 28, No. 3, pp. 518–564, September 1996.

9. "Verifying a Logic-Synthesis Algorithm and Implementation: A Case Study in Software Verification," Mark Aagaard and Miriam Leeser. *IEEE Transactions on Software Engineering*, Vol. 21 No. 10, pp. 822–833, October 1995.

8. "An Automaton Model for Scheduling Constraints," Andrés Takach, Wayne Wolf, and Miriam Leeser. *IEEE Transactions on Computers*, Vol. 44 No. 1, pp. 1–12, January 1995.

7. "A Methodology for Efficient Hardware Verification," Mark Aagaard and Miriam Leeser. *Journal of Formal Methods in System Design*, Vol. 5 Nos 1/2, pp. 95–117, July 1994.

6. "PBS: Proven Boolean Simplification," Mark Aagaard and Miriam Leeser. *IEEE Transactions on Computer-Aided Design*, Vol. 13 No. 4, pp. 459–470, April, 1994.

5. "High Level Synthesis and Generating FPGAs with the BEDROC System," Miriam Leeser, Richard Chapman, Mark Aagaard, Mark Linderman, and Stephan Meier. *Journal of VLSI Signal Processing*, Vol. 6 No. 2, pp. 191–214, 1993.

4. "Using Nuprl for the Verification and Synthesis of Hardware," Miriam Leeser. *Philosophical Transactions of the Royal Society, A*. Vol. 339, pp. 49–68, 1992.

3. "Formally Verified Synthesis of Combinational CMOS Circuits," David A. Basin, Geoffrey M. Brown, and Miriam Leeser. *Integration, the VLSI Journal*, Vol. 11, pp. 235–250, 1991.

2. "Reasoning about the Function and Timing of Integrated Circuits with Interval Temporal Logic," Miriam Leeser. *IEEE Transactions on Computer-Aided Design*, Vol. 8 No. 12, pp. 1233–1246, December 1989.

1. "Automatic Determination of Signal Flow through MOS Transistor Networks," W. F. Clocksin and M. E. Leeser. *Integration, the VLSI Journal*, Vol. 4, pp. 53–63, 1986.

Editorials

3. "Guest Editor's Introduction," Miriam Leeser and Vinay Sriram. *EURASIP Journal on Embedded Systems Special Issue on FPGA Supercomputing Platforms, Architectures and Techniques for Accelerating Computationally Complex Algorithms.* Volume 2009.

2. "Special Issue: General-purpose Processing using Graphics Processing Units," David Kaeli and Miriam Leeser. *Journal Parallel and Distributed Computing*, pp. 1305-1306, Oct. 2008.

1. "Field-Programmable Gate Arrays in Embedded Systems," Miriam Leeser, Scott Hauck, and Russell Tessier. Eurasip Journal on Embedded Systems, Volume 2006.

Refereed Conference Papers

98. "Scaling Neural Network Performance through Customized Hardware Architectures on Reconfigurable Logic," Michaela Blott, Thomas Preußer, Nicholas Fraser, Giulio Gambardella, Kenneth O'Brien, Yaman Umuroglu, and Miriam Leeser. *35th IEEE International Conference on Computer Design (ICCD)*, November 2017.

97. "Accelerating Big Data Applications Using Lightweight Virtualization Framework on Enterprise Cloud," Janki Bhimani, Zhengyu Yang, Miriam Leeser and Ningfang Mi. *Twenty-first IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2017.

96. "FPGA Modeling Techniques for Detecting and Demodulating Multiple Wireless Protocols," Benjamin Drozdenko, Suranga Handagala, Kaushik Chowdhury, and Miriam Leeser. *23rd International Conference on Field Programmable Logic and Applications (FPL)*, August 2017.

95. "FIM: Performance Prediction for Parallel Computation in Iterative Data Processing Applications," Janki Bhimani, Ningfang Mi, Miriam Leeser and Zhengyu Yang. *10th IEEE International Conference on Cloud Computing (IEEE CLOUD 2017)*, June, 2017.

94. "Using High Level GPU Tasks to Explore Memory and Communications Options on Heterogeneous Platforms," Chao Liu, Janki Bhimani and Miriam Leeser. *Software Engineering Methods for Parallel and High Performance Applications (SEM4HPC)*, June 2017.

93. "Secure Function Evaluation Using an FPGA Overlay Architecture," Xin Fang, Stratis Ioannidis, and Miriam Leeser. *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*. Feb. 2017.

92. "A Framework for Developing Parallel Applications with high level Tasks on Heterogeneous Platforms," Chao Liu and Miriam Leeser. *8th ACM International Workshop on Programming Models and Applications for Multicores and Manycores (PMAM)*. Feb. 2017.

91. "Performance Prediction Techniques for Scalable Large Data Processing in Distributed MPI Systems," Janki Bhimani, Ningfang Mi, Miriam Leeser and Zhengyu Yang. *35th IEEE International Performance Computing and Communications Conference (IPCCC)*. December 2016.

90. "Design space exploration of GPU Accelerated cluster systems for optimal data transfer using PCIe bus," Janki Bhimani, Miriam Leeser, Ningfang Mi. *Twentieth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2016.

89. "Unified and lightweight tasks and conduits: A high level parallel programming framework," Chao Liu and Miriam Leeser. *Twentieth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2016.

88. "Modeling Considerations for the Hardware-Software Co-design of Flexible Modern Wireless Transceivers," Benjamin Drozdenko, Matthew Zimmermann, Tuan Dao, Kaushik Chowdhury, and Miriam Leeser. *22nd International Conference on Field Programmable Logic and Applications (FPL)*, August 2016.

87. "State-action based Link Layer Design for IEEE 802.11b Compliant MATLAB-based SDR," R. Subramanian, E. Doyle, B. Drozdenko, M. Leeser and K. R. Chowdhury. *IEEE Distributed Computing in Sensor Systems*, May 2016.

86. "Cardiac MRI compressed sensing image reconstruction with a graphics processing unit," Majid Sabbagh, Martin Uecker, Andrew J. Powell, Miriam Leeser, and Mehdi H. Moghari. *International Symposium on Medical Information and Communication Technology (ISMICT)*, March 2016.

85. "Accelerating K-Means Clustering with Parallel Implementations and GPU computing," Janki Bhimani, Miriam Leeser, Ningfang Mi. *Nineteenth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2015.

84. "GPU Implementation of Reverse Coordinate Conversion for Proteins," Mahsa Bayati, Jaydeep P. Bardhan, Miriam Leeser. *Nineteenth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2015.

83. "Leakage Evaluation on Power Balance Countermeasure Against Side-Channel Attack on FPGAs," Xin Fang, Pei Luo, Yunsi Fei, and Miriam Leeser. *Nineteenth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2015.

82. "Behavioral Non-portability in Scientific Numeric Computing," Y. Gu, T. Wahl, M. Bayati and M. Leeser. *Euro-Par International Conference on Parallel and Distributed Computing*, pp. 558–569, August 2015.

81. "Side-channel Analysis of MAC-Keccak Hardware Implementations," P. Luo, Y.Fei, X. Fang, A. Ding, D. Kaeli, and M. Leeser. *Hardware and Architectural Support for Security and Privacy*, June 2015.

80. "Implementing a MATLAB-based Self-Configurable Software-Defined Radio Transceiver," Benjamin Drozdenko, Ramanathan Subramanian, Kaushik Chowdhury, and Miriam Leeser. *10th International Conference on Cognitive Radio Oriented Wireless Networks (CROWNCOM)*. pp. 164-175. April, 2015.

79. "Power Analysis Attack on Hardware Implementation of MAC-Keccak on FPGAs," Pei Luo, Yunsi Fei, Xin Fang, A. Adam Ding, Miriam Leeser and David R. Kaeli. *International Conference on ReConFigurable Computing and FPGAs*, Cancun, Mexico. December 2014.

78. "Accelerating Protein Coordinate Conversion using GPUs," Mahsa Bayati, Jaydeep Bardhan, D. M. King and Miriam Leeser. *Eighteenth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2014.

77. "Reducing Processing Latency with a Heterogeneous FPGA-Processor Framework," J. Pendlum, M. Leeser and K. Chowdhury. *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2014.

76. "Make it real: Effective floating-point reasoning via exact arithmetic, " Miriam Leeser, Saoni Mukherjee, Jaideep Ramachandran and Thomas Wahl. *Design, Automation & Test in Europe Conference (DATE)*, March 2014.

75. "FPGA-based Hyperspectral Covariance Coprocessor for Size, Weight, and Power," David Kusinsky and Miriam Leeser. *Seventeenth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2013.

74. "Vendor Agnostic, High Performance, Double Precision Floating Point Division for FPGAs," Xin Fang and Miriam Leeser. *Seventeenth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2013. (Runner up, Best Poster Award.)

73. "Kernel Specialization for Improved Adaptability and Performance on Graphics Processing Units (GPUs)," Nicholas Moore, Miriam Leeser and Laurie Smith King. *27th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*. pp. 1037–1048. May 2013.

72. "Minimum Energy Operation for Clustered Island-Style FPGAs," Peter Grossmann, Miriam Leeser and Marvin Onabajo. *21st ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2013. pp. 157-166.

71. "Characterization of a Single-Supply Subthreshold FPGA," Peter Grossmann, Miriam Leeser, and Marvin Onabajo. *IEEE Subthreshold Microelectronics Conference*. October 2012.

70. "CUDA and OpenCL Implementations of 3D CT Reconstruction for Biomedical Imaging," Saoni Mukherjee, Nicholas Moore, James Brock and Miriam Leeser. *Sixteenth IEEE High-Performance Extreme Computing Conference (HPEC)*. September 2012.

69. "CRUSH: Cognitive Radio Universal Software Hardware," George Eichinger, Kaushik Chowdhury and Miriam Leeser. *22nd International Conference on Field Programmable Logic and Applications (FPL)*, August 2012.

68. "OpenCL Floating Point Software on Heterogeneous Architectures –Portable or Not?," Miriam Leeser, Jaideep Ramachandran, Thomas Wahl, and Devon Yablonski. *Fifth International Workshop on Numerical Software Verification (NSV)*. July 2012.

67. "Heterogeneous Tasks and Conduits Framework for Rapid Application Portability and Deployment," J. Brock, M. Leeser and M. Niedre. *Innovative Parallel Computing*, May 2012.

66. "Incremental Clustering Applied to Radar Deinterleaving: A Parameterized FPGA Implementation," S. Bailie and M. Leeser. *20th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2012. pp. 25–28.

65. "Circuit-Level Considerations for an Ultra-Low Voltage FPGA with Unidirectional, Single-Driver Routing Fabric," Peter Grossmann and Miriam Leeser. *IEEE Subthreshold Microelectronics Conference*. September 2011.

64. "Adaptable Two-Dimension Sliding Windows on NVIDIA GPUs with Runtime Compilation," Nicholas Moore, Miriam Leeser and Laurie Smith King. *Symposium on Application Accelerators in High Performance Computing (SAAHPC)*, pp. 103 – 112. July 2011. *Winner, Best Paper Award.*

63. "An Autonomous Vector/Scalar Floating Point Coprocessor for FPGAs," J. Kathiara and M. Leeser. *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2011.

62. "Accelerating Algorithms on GPUs in SCIRun: the Conjugate Gradient Case Study," D. Yablonski, M. Leeser and D. Brooks. *Symposium on Application Accelerators in High Performance Computing (SAAHPC)*, July 2010.

61. "Efficient Template Matching with Variable Size Templates in CUDA," N. Moore, M. Leeser and L. Smith King. *IEEE Symposium on Application Specific Processors (SASP)*, June 2010.

60. "Accelerating phase unwrapping and affine transformations for optical quadrature microscopy using CUDA," P. Mistry, S. Braganza, D. Kaeli and M. Leeser, 2nd Workshop on General Purpose Processing on Graphics Processing Units, pp. 28-37. ACM, 2009.

59. "The Effect of Parameterization on a Reconfigurable Implementation of PIV," A. Bennis, M. Leeser and G. Tadmor. *Engineering of Reconfigurable Systems and Algorithms (ERSA)*, July 2009.

58. "Implementing a Highly Parameterized Digital PIV System On Reconfigurable Hardware," A. Bennis, M. Leeser and G. Tadmor. *IEEE International Conference Application-specific Systems, Architectures and Processors (ASAP)*, July 2009.

57. "Two-Dimensional Phase Unwrapping on FPGAs and GPUs," Sherman Braganza and Miriam Leeser. *Workshop on High-Performance Reconfigurable Computing Technology and Applications (HPRCTA'08)*. November 2008.

56. "An Efficient Implementation Of A Phase Unwrapping Kernel On Reconfigurable Hardware", Sherman Braganza and Miriam Leeser. *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2008)*, July 2008.

55. "An FPGA Implementation of Explicit-State Model Checking," M. E. Fuess, M. Leeser and T. Leonard. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 119 - 126, April 2008.

54. "The 1D Discrete Cosine Transform For Large Point Sizes Implemented On Reconfigurable Hardware", Sherman Braganza and Miriam Leeser. *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2007)*, July 2007.

53. "K-means Clustering for Multispectral Images Using Floating-Point Divide," X. Wang and M. Leeser. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 151 - 162, April 2007.

52. "Writing Portable Applications that Dynamically Bind at Run Time to Reconfigurable Hardware," N. Moore, A. Conti M. Leeser and L. Smith King. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 229 - 238 April 2007.

51. "Efficient use of Communications Between an FPGA's Embedded Processor and its Reconfigurable Logic," Joshua Noseworthy and Miriam Leeser. *Engineering of Reconfigurable Systems and Algorithms (ERSA)*, pp. 191–197. June 2006.

50. "Advanced Components in the Variable Precision Floating-Point Library," Xiaojun Wang, Sherman Braganza and Miriam Leeser. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM2006)*, pp. 249–258. April 2006.

49. "Automatic Sliding Window Operation Optimization for FPGA-Based Computing Boards," Haiqian Yu and Miriam Leeser. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 76–88. April 2006.

48. "Optimizing Data Intensive Window-Based Image Processing on Reconfigurable Hardware Boards," Haiqian Yu and Miriam Leeser. *IEEE 2005 Workshop on Signal Processing Systems (SIPS)*. November 2005.

47. "Enabling a Real-Time Solution for Neuron Detection with Reconfigurable Hardware," Ben Cordes, Jennifer Dy, Miriam Leeser and James Goebel. *16th IEEE International Workshop on Rapid System Prototyping*, pp. 128–134, June 2005.

46. "Dynamo, a Run-Time Partitioning System," L. A. Smith King, Miriam Leeser, Heather Quinn. *Engineering of Reconfigurable Systems and Algorithms (ERSA)*, pp. 145–151. June 2004.

45. "Smart Camera Based on Reconfigurable Hardware Enables Diverse Real-time Applications," Miriam Leeser, Shawn Miller and Haiqian Yu. *IEEE Symposium on Field-Programmable Custom Computing Machines FCCM)*, pp. 147–155. April 2004.

44. "An FPGA Implementation of the Two-Dimensional Finite-Difference Time-Domain (FDTD) Algorithm ," Wang Chen, Panos Kosmas, Miriam Leeser and Carey Rappaport. *Twelfth ACM International Symposium on Field-Programmable Gate Arrays (FPGA2004)*, pp. 213–222. February 2004.

43. "Precision Modeling of Floating-Point Applications for Variable Bitwidth Computing," Zhihong Zhao and Miriam Leeser. *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, pp. 208–214. June 2003.

42. "Runtime Assignment of Reconfigurable Hardware Components for Image Processing Pipelines," Heather Quinn, L. A. Smith King, Miriam Leeser, Waleed Meleis. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 173–182. April 2003.

41. "A Library of Parameterized Floating Point Modules and Their Use," Pavle Belanovic and Miriam Leeser. *12th International Conference on Field Programmable Logic and Application (FPL)*, pp. 657–666. September 2002.

40. "Parallel-Beam Backprojection: an FPGA Implementation Optimized for Medical Imaging," Srdjan Coric, Miriam Leeser, Eric Miller, Marc Trepanier. *Tenth ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 217–226. February 2002.

39. "Runtime Execution of Reconfigurable Hardware in a Java Environment," L. A. Smith King, H. Quinn, M. Leeser, D. Galatopoullos, E. Manolakos. In *International Conference on Computer Design (ICCD)*, pp. 380–385. September 2001.

38. "Applying Reconfigurable Hardware to the Analysis of Multispectral and Hyperspectral Imagery," M. Leeser, P. Belanovic, M. Estlick, M. Gokhale, J. Szymanski, J. Theiler. *Imaging Spectrometry VII*, Proceedings of SPIE Vol. 4480, pp. 100–107. August, 2001.

37. "Algorithmic Transformations in the Implementation of K-means Clustering on Reconfigurable Hardware," Mike Estlick, Miriam Leeser, James Theiler, John J. Szymanski. *Ninth ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 103–110. February 2001.

36. "Effect of Data Truncation in an Implementation of Pixel Clustering on a Custom Computing Machine," M. Leeser, J. Theiler, M. Estlick, N. Kitaryeva, J. Szymanski. *Reconfigurable Technology for Computing and Applications II*, Proceedings of SPIE Vol. 4212, pp. 80–89, September 2000.

35. "Design Issues for Hardware Implementation of an Algorithm for Segmenting Hyperspectral Imagery," James Theiler, Miriam Leeser, Michael Estlick, and John J. Szymanski. *Image Spectrometry VI*, Proceedings of SPIE Vol. 4132, pp. 99–106, July 2000.

34. "Design Tradeoffs in a Hardware Implementation of the K-Means Clustering Algorithm," Miriam Leeser, James Theiler, Michael Estlick and John J. Szymanski. *First IEEE Sensor Array and Multichannel Signal Processing Workshop (SAM2000)*, pp. 520–524, March 2000.

33. "Implementing a RAKE Receiver for Wireless Communications on an FPGA-based Computer System," Ali M. Shankiti and Miriam Leeser. *Eighth ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*. pp. 145–151, February 2000.

32. "Adaptive Motor Control with Reconfigurable Logic," Miriam Leeser and Karen Matulis. *Reconfigurable Technology: FPGAs for Computing and Applications*, Proceedings of SPIE Vol. 3844, pp. 122–128, September 1999.

31. "Integrating Floorplanning In Data-Transfer Based High-Level Synthesis," Shantanu Tarafdar, Miriam Leeser and Zixin Yin. *IEEE/ACM International Conference on CAD*, pp. 412–417, November 1998.

30. "Spatial and Color Clustering on an FPGA based Computer System," Miriam Leeser, Natasha Kitaryeva, and Jill Crisman. *Voice, Video and Data Communications, Photonics East 98*, SPIE Vol. 3526, pp. 25–33, November 1998.

29. "Enabling MPEG-2 Video Playback in Embedded Systems Through Improved Data Cache Efficiency," Peter Soderquist and Miriam Leeser. *Voice, Video and Data Communications, Photonics East 98*, SPIE Vol. 3528, pp. 225–236, November 1998.

28. "The DT-Model: High-Level Synthesis Using Data Transfers," Shantanu Tarafdar and Miriam Leeser. *35th ACM/IEEE Design Automation Conference*, pp. 114–117, June 1998.

27. "Truly Rapid Prototyping Requires High Level Synthesis," Goran Doncev, Miriam Leeser and Shantanu Tarafdar. *9th IEEE International Workshop on Rapid System Prototyping*, pp. 101–106, June 1998.

26. "Optimizing the Data Cache Performance of a Software MPEG-2 Video Decoder," Peter Soderquist and Miriam Leeser. In *ACM Multimedia*, pp. 291–301, November 1997.

25. "Memory Traffic and Data Cache Behavior of an MPEG-2 Software Decoder," Peter Soderquist and Miriam Leeser. In *International Conference on Computer Design (ICCD)*, pp. 417–422, October 1997.

24. "Architectural Design of a Three Dimensional FPGA," Waleed Meleis, Miriam Leeser, Paul Zavracky and Mankuan Vai. In *17th Conference on Advanced Research in VLSI (ARVLSI)*, pp. 256–268, September 1997.

23. "Rothko: A Three Dimensional FPGA Architecture, its Fabrication, and Design Tools," Miriam Leeser Waleed Meleis, Mankuan Vai, and Paul Zavracky. In P. Cheung, W. Luk, and M. Glessner, editors, *Field Programmable Logic and Applications*. Springer-Verlag Lecture Notes in Computer Science No. 1304. pp. 21–30, 1997.

22. "Rapid Prototyping of Datapath Intensive Architectures with HML, an Abstract Hardware Description Language," Miriam Leeser, Shantanu Tarafdar and Yanbing Li. High-Speed Computing, Digital Signal Processing, and Filtering using Reconfigurable Logic, SPIE Vol. 2914, pp. 259–270, November 1996.

21. "From Abstract Specification to Field Programmable Hardware with HML," Miriam Leeser, Shantanu Tarafdar and Yanbing Li. In *Cornell Workshop on Hardware Synthesis and Verification*, August 1996.

20. "Verification of a Subtractive Radix-2 Square Root Algorithm and Implementation," Miriam Leeser and John O'Leary. In *IEEE International Conference on Computer Design*, pp. 526–531, October 1995.

19. "HML: An Innovative Hardware Description Language and Its Translation to VHDL," Yanbing Li and Miriam Leeser. *Proceedings, IFIP International Conference on Computer Hardware Description Languages and their Applications*, pp. 691–696, August 1995.

18. "An Area/Performance Comparison of Subtractive and Multiplicative Divide/Square Root Implementations," Peter Soderquist and Miriam Leeser. In 12^{th} *IEEE Symposium on Computer Arithmetic*, pp. 132–139, July 1995.

17. "Non-Restoring Integer Square Root: A Case Study in Design by Principled Optimization," John O'Leary, Miriam Leeser, Jason Hickey and Mark Aagaard. *International Conference on Theorem Provers in Circuit Design*, October 1994. Published in Vol. 901 of Lecture Notes in Computer Science, (T. Kropf and R. Kumar, eds.), pp. 52–71, Springer Verlag, 1995.

16. "Reasoning about Pipelines with Structural Hazards," Mark Aagaard and Miriam Leeser. *International Conference on Theorem Provers in Circuit Design*, October, 1994. Published in Vol. 901 of Lecture Notes in Computer Science, (T. Kropf and R. Kumar, eds.), pp. 13–32, Springer Verlag, 1995.

15. "Simulation of Digital Circuits in the Presence of Uncertainty," Mark Linderman and Miriam Leeser. *1994 IEEE International Conference on Computer-Aided Design*, pp. 248–251, November 1994.

14. "Toward a Super Duper Hardware Tactic," Mark Aagaard, Miriam Leeser and Phillip Windley. In Jeffrey Joyce and Carl-Johan Seger, eds, *Higher Order Logic Theorem Proving and its Applications*. Springer-Verlag Lecture Notes in Computer Science No 780, pp. 399–412, 1994.

13. "A Framework for Specifying and Designing Pipelines," Mark Aagaard and Miriam Leeser. *Proceedings, IEEE International Conference on Computer Design*, IEEE Computer Society Press, pp. 548–551, October 1993.

12. "Implementing Floating-Point Square Root Computation with Newton's Method," Peter Soderquist and Miriam Leeser. In *International Workshop on Hardware-Software Co-design*. Cambridge, MA, October 1993.

11. "HML: A Hardware Description Language Based on SML," John O'Leary, Mark Linderman, Miriam Leeser and Mark Aagaard. In D. Agnew, L. Claesen and R. Camposano, eds, *IFIP Conference on Hardware Description Languages and their Applications*, pp. 313–320, April 1993.

10. "Verifying a Logic Synthesis Tool in Nuprl: A Case Study in Software Verification," Mark Aagaard and Miriam Leeser. *Workshop on Computer Aided Verification (CAV)*. June 1992.

9. "Verified High-Level Synthesis in BEDROC," Richard Chapman, Geoffrey Brown and Miriam Leeser. *European Conference on Design Automation (EDAC)*, pp. 59–63, March 1992.

8. "A Formally Verified System for Logic Synthesis," Mark Aagaard and Miriam Leeser. *IEEE International Conference on Computer Design*, pp. 346–350, October 1991.

7. "The BEDROC High Level Synthesis System," Miriam Leeser, Mark Aagaard, Mark Linderman, Richard Chapman, Richard Johnson and Stephan Meier. *IEEE International ASIC Conference and Exhibit*, pp. 2-5.1 – 2-5.5, September 1991.

6. "EDISYN: A Language-Based Editor for High-Level Synthesis," Chee-Keng Chang, Geoffrey Brown and Miriam Leeser. In D. Borrione and R. Waxman, eds, *Computer Hardware Description Languages and their Applications*, North-Holland, pp. 371–389, April, 1991.

5. "Hardware Scheduling with Real-Time A* Search," Miriam Leeser and Stephan Meier. *Fifth International Workshop on High-Level Synthesis*, Germany, March 1991.

4. "Preserving Design Behavior without Register-Transfer Equivalence," Miriam Leeser and Wayne Wolf. *Fifth International Workshop on High-Level Synthesis*, Germany, March 1991.

3. "Behavior FSMs for High-Level Verification and Synthesis," Miriam Leeser and Wayne Wolf. *ACM Workshop on Formal Methods in VLSI Design*, Miami FL, January 1991.

2. "Synthesizing Correct Sequential Circuits," Geoffrey Brown and Miriam Leeser. In J. A. Darringer and F. J. Rammig, eds, *International Conference on Computer Hardware Description Languages*, North-Holland, pp. 169–182, January 1990.

1. "Verifying High-Level Hardware Synthesis Tools," Miriam Leeser and Geoffrey Brown. in *Fourth International Workshop on High-Level Synthesis*, October 1989.

Posters and other Refereed Papers Conferences, Workshops and Symposia

66. "Identifying Volatile Numeric Expressions in OpenCL Applications," Mahsa Bayati, Brian Crafton, Miriam Leeser, Yijia Gu and Thomas Wahl. *Numerical Reproducibility at Exascale*, Workshop at SuperComputing, November 2016.

65. "Garbled Circuits for Preserving Privacy in the Datacenter," Xin Fang, Stratis Ioannidis and Miriam Leeser. *Heterogeneous High Performance Reconfigurable Computing (H2RC) Workshop.* Nov, 2016.

64. "High-Level Hardware-Software Co-design of an 802.11a Transceiver System using Zynq SoC," B. Drozdenko, M. Zimmermann, T. Dao, M. Leeser and K. R. Chowdhury, *IEEE INFOCOM*, Apr. 2016.

63. "Balance Power Leakage to Fight Against Side-Channel Analysis at Gate Level in FPGAs," Xin Fang, Pei Luo, Yunsi Fei and Miriam Leeser. *IEEE ASAP conference*, July 2015.

62. "Full Duplex 802.11a-Compliant Transceiver with Split Functionalities," Rahman Doost, Benjamin Drozdenko, Kaushik Chowdhury, and Miriam Leeser. *New England Workshop on Software Defined Radio (NEWSDR)*, May 2015.

61. "Bi-Directional Transceiver Implementation with Optimal Parameter Selection," Benjamin Drozdenko, Ramanathan Subramanian, Kaushik Chowdhury, and Miriam Leeser. *New England Workshop on Software Defined Radio (NEWSDR)*, May 2015.

60. "Accuracy of kinect for measuring shoulder joint angles in multiple planes of motion," Meghan Huber, Miriam Leeser, Dagmar Sternad, and Amee Seitz. *IEEE International Conference on Virtual Rehabilitation (ICVR)*, 2015.

59. "Predicting the Performance of Machine Learning Algorithms running on Heterogeneous Computing Platforms," Janki Bhimani, Miriam Leeser and Ningfang Mi. *Women in Machine Learning Workshop.* December 2014.

58. "Accuracy and Precision of a Low-Cost Virtual Rehabilitation System Utilizing the Microsoft Kinect to Measure Shoulder Motion." A. L. Seitz, M. Huber, M. Leeser, and D. Sternad *American Society of Shoulder and Elbow Therapists Annual Meeting*, Pinehurst, North Carolina Oct, 2014.

57. "CRASH: Cognitive Radio Accelerated with Software and Hardware," Jonathon Pendlum, Miriam Leeser, and Frank Bruno. *New England Workshop on Software Defined Radio*, May 2014.

56. "PHY and Link Layer SDR Implementation Using MATLAB," Benjamin Drozdenko, Jingzhi Yu, Kaushik Chowdhury, and Miriam Leeser. *New England Workshop on Software Defined Radio*, May 2014.

55. "Validity and Reliability of Kinect for Measuring Shoulder Joint Angles," M.E. Huber, AL Seitz, M. Leeser and D. Sternad. *IEEE Proceedings of the 40th Northeast Bioengineering Conference.* April 2014. Runner up, best student poster award.

54. "GPGPU Computing for Clouds and Smartphones," Virginia Ross and Miriam Leeser. *AFRL Technical Interchange Meeting: Use of Accelerators for Signal Processing with an Emphasis on Synthetic Aperture Radar (SAR).* April 2014.

53. "Development of a low-cost, adaptive, clinician-friendly virtual rehabilitation system," M. E. Huber and M. Leeser and D. Sternad. *International Conference on Virtual Rehabilitation.* August, 2013. **Winner Best Student Poster Award.**

52. "Cognitive Radio Universal Software Hardware," G. Eichinger, K. R. Chowdhury and M. Leeser. it Proc. of IEEE DySPAN, demonstration session. October, 2012.

51. "Cognitive Radio Universal Software Hardware," George Eichinger, Kaushik Chowdhury, Miriam Leeser. *Field Programmable Custom Computing Machines (FCCM)*, April 2012.

50. "Implementing Murphi: Accelerating Large State Space Exploration on FPGAs," Mary Ellen Tie and Miriam Leeser. *Field Programmable Custom Computing Machines (FCCM)*, April 2012.

49. "An FPGA Spectrum Sensing Accelerator for Cognitive Radio," George Eichinger, Miriam Leeser and Kaushik Chowdhury. *Fifteenth Annual Workshop on High-Performance Embedded Computing (HPEC).* September 2011.

48. "FPGA-based Acceleration of Hyperspectral K-Means Clustering," David Kusinsky and Miriam Leeser. *Fifteenth Annual Workshop on High-Performance Embedded Computing (HPEC).* September 2011.

47. "A Prototype FPGA for Subthreshold-Optimized CMOS," Peter Grossmann and Miriam Leeser. *Nineteenth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2011).* February 2011.

46. "Sparse Matrix Algorithms on GPUs and their Integration into SCIRun," Devon Yablonski, Miriam Leeser and Dana Brooks. *Fourteenth Annual Workshop on High-Performance Embedded Computing (HPEC).* September 2010.

45. "Adaptable and Efficient Variable Size Template Matching in CUDA," Nicholas Moore, Miriam Leeser and Laurie Smith King. *Fourteenth Annual Workshop on High-Performance Embedded Computing (HPEC).* September 2010.

44. "Adding support for GPUs to PVTOL: The Parallel Vector Tile Optimizing Library," James Brock, Miriam Leeser and Mark Niedre. *Fourteenth Annual Workshop on High-Performance Embedded Computing (HPEC).* September 2010.

43. "An FPGA Implementation of Incremental Clustering for Radar Pulse Deinterleaving," Scott Bailie and Miriam Leeser. *Fourteenth Annual Workshop on High-Performance Embedded Computing (HPEC).* September 2010.

42. "A Prototype FPGA Tile for Subthreshold-Optimized CMOS," Peter Grossmann and Miriam Leeser. *Fourteenth Annual Workshop on High-Performance Embedded Computing (HPEC).* September 2010.

41. "Using Variable Precision Floating Point with Embedded Hard and Soft Core Processors," J. Kathiara, M. Leeser and P. Palana. *Field Programmable Custom Computing Machines (FCCM)*, May 2010.

40. "Adapting the USRP as an Underwater Acoustic Modem," Paul Ozog, Miriam Leeser and Milica Stojanovic. *Thirteenth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2009.

39. "Accelerating a MATLAB Application with Nvidia GPUs: a Case Study for GPU Library Construction," Nicholas Moore and Miriam Leeser. *Thirteenth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2009.

38. "Accelerating Explicit State Model Checking on FPGAs: PHAST, " Mary Ellen Tie and Miriam Leeser. *International Conference on Formal Methods and Models for Codesign (MEMOCODE)*. July 2009.

37. "2D Phase Unwrapping on FPGAs and GPUs," Sherman Braganza and Miriam Leeser. *Twelfth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2008.

36. "Extending VForce to Include Support for NVIDIA GPUs using CUDA," Dennis Cuccaro, Nicholas Moore, Miriam Leeser and Laurie Smith King. *Twelfth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2008.

35. "Implementation of a Highly Parameterized Digital PIV System On Reconfigurable Hardware," Abderrahmane Bennis, Miriam Leeser, Gilead Tadmor, Russ Tedrake. *Twelfth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2008.

34. "Efficient FPGA Implementation of QR Decomposition Using a Systolic Array Architecture," Xiaojun Wang and Miriam Leeser. *International Conference on Field Programmable Gate Arrays (FPGA)*. February 2008.

33. "Phase Unwrapping On Reconfigurable Hardware," Sherman Braganza and Miriam Leeser. *Eleventh Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2007.

32. "FPGA Based Systolic Array Implementation of QR Transformation Using Givens Rotations," Xiaojun Wang and Miriam Leeser. *Eleventh Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2007.

31. "Vforce: Aiding the Productivity and Portability in Reconfigurable Supercomputer Applications via Runtime Hardware Binding," Nicholas Moore, Miriam Leeser and Laurie Smith King. *Eleventh Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2007. *Best paper award winner.*

30. "Performance Tuning on Reconfigurable Supercomputers: A Case Study," Ben Cordes, Albert Conti, Miriam Leeser, and Eric Miller. Poster abstract, in *Supercomputing (SC'06)*. November 2006.

29. "Improving the Performance of Parallel Backprojection on a Reconfigurable Supercomputer," Ben Cordes, Miriam Leeser, Eric Miller and Richard Linderman. *Tenth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2006.

28. "Heterogeneous Processing Element Support for VSIPL++," Al Conti, Miriam Leeser, Nicholas Moore and Laurie Smith-King. *Tenth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2006.

27. "VSIPL++ Support for Programming Reconfigurable Supercomputers," Nicholas Moore, Ben Cordes, Albert Conti, Miriam Leeser, Laurie Smith-King. *Reconfigurable Systems Summer Institute (RSSI)*. July 2006.

26. "Acceleration of the 3D FDTD Algorithm in Fixed-point Arithmetic using Reconfigurable Hardware," Wang Chen, Miriam Leeser, and Carey Rappaport. *Progress in Electromagnetics Research Symposium (PIERS 2006)*. March 2006.

25. "Efficient use of Communications Between an FPGA's Embedded Processor and its Reconfigurable Logic," Joshua Noseworthy and Miriam Leeser. In *Fourteenth ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*. Poster abstract. February 2006.

24. "An FPGA API for VSIPL++," Ben Cordes, Miriam Leeser, and Joe Tarkoff. *Ninth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2005.

23. "Adapting Parallel Backprojection to an FPGA Enhanced Distributed Computing Environment," Albert A. Conti, Ben Cordes, Miriam Leeser, Eric Miller and Richard Linderman. *Ninth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2005.

22. "Interface Techniques for Microprocessors Embedded Within FPGAs," Joshua Noseworthy and Miriam Leeser. *Ninth Annual Workshop on High-Performance Embedded Computing (HPEC)*. September 2005.

21. "Accelerating Backprojection for SAR on an HHPC with FPGAs," A. Conti, B. Cordes, M. Leeser, and. Eric Miller. *Bishop's Lodge Workshop in Distributed Embedded Computing*, June 2005.

20. "Enabling a Real-Time Solution for Neuron Detection with Reconfigurable Hardware," Ben Cordes, Jennifer Dy, Miriam Leeser and James Goebel. *ACM/SIGDA Thirteenth International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2005.

19. "Real-Time Particle Image Velocimetry for Feedback Loops Using FPGA Implementation," H. Yu, M. Leeser, G. Tadmor, and S. Siegel. *43rd AIAA Aerospace Sciences Meeting and Exhibit*, January 2005.

18. "Variable Precision Floating Point Division and Square Root," Miriam Leeser and Xiaojun Wang. *Eighth Annual Workshop on High Performance Embedded Computing (HPEC)*, pp. 47–48. September 2004.

17. "Dynamo: A Runtime Codesign Environment," Heather Quinn, Miriam Leeser and L. A. Smith King. *Eighth Annual Workshop on High Performance Embedded Computing (HPEC)*, pp. 65–66. September 2004.

16. "A Parameterized Floating-Point Library Applied to Multispectral Image Clustering," Xiaojun Wang, Miriam Leeser and Haiqian Yu. *Military and Aerospace Programmable Logic Devices (MAPLD)*. September 2004.

15. "Multimedia Macros for Portable Optimized Programs," Juan Carlos Rojas and Miriam Leeser. *Seventh Annual Workshop on High Performance Embedded Computing (HPEC)*, pp. 213–214. September 2003.

14. "An FPGA Implementation of Two-Dimensional Finite-Difference Time-Domain (FDTD) Algorithm," Wang Chen, Panos Kosmas, Miriam Leeser and Carey Rappaport. *Seventh Annual Workshop on High Performance Embedded Computing (HPEC)*, pp. 105–106. September 2003.

13. "Acceleration of the Retinal Vascular Tracing Algorithm Using FPGAs," Shawn Miller and Miriam Leeser. *Seventh Annual Workshop on High Performance Embedded Computing (HPEC)*, pp. 133–134. September 2003.

12. "Precision Modeling and Bit-Width Optimization of Floating-Point Applications," Zhihong Zhao and Miriam Leeser. *Seventh Annual Workshop on High Performance Embedded Computing (HPEC)*, pp. 141–142. September 2003.

11. "Portable FPGA Designs with Interface Adaptive Module," Haiqian Yu and Miriam Leeser. *Military and Aerospace Programmable Logic Devices (MAPLD)*. September 2003.

10. "A Library of Parameterized Hardware Modules for Floating-Point Arithmetic and Its Use," Pavle Belanovic and Miriam Leeser. *Sixth Annual Workshop on High Performance Embedded Computing (HPEC)*, pp. 45–46. September 2002.

9. "Implementing Image Processing Pipelines in a Hardware / Software Environment," Heather Quinn, Miriam Leeser, and Laurie Smith King. *Sixth Annual Workshop on High Performance Embedded Computing (HPEC)*, pp. 29–31. September 2002.

8. "Accelerating Image Processing Pipelines in a Hardware/Software Environment," Heather Quinn, Miriam Leeser, and Laurie Smith King. *Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2002.

7. "Parameterized K-means Clustering for Rapid Hardware Development to Accelerate Analysis of Satellite Data," Miriam Leeser, Pavle Belanovic, Michael Estlick, Maya Gokhale, John Szymanski, and James Theiler. *High Performance Embedded Computing (HPEC)*, November 2001.

6. "Employing Reconfigurable Hardware in a Networked Environment," M. Leeser, H. Quinn, L. A. Smith King. *Fifth Annual Workshop on High Performance Embedded Computing (HPEC)*, November 2001.

5. "Applying Reconfigurable Hardware to Segmentation for Multispectral Imagery," Miriam Leeser, Michael Estlick, Natasha Kitaryeva, John Szymanski, and James Theiler. *High Performance Embedded Computing (HPEC)*, September 2000.

4. "Software Support for the Integration of Reconfigurable Computing with Networks of Workstations," M. Leeser , R. Porter, and E. S. Manolakos. *Proceedings of the Military and Aerospace Applications of Programmable Devices and Technologies (MAPLD)*, September 2000.

3. "High-Level Design Space Tradeoffs for Implementing a RAKE Receiver on an FPGA-based Computer System," Ali Shankiti and Miriam Leeser. *Boston Synopsys Users Group Meeting*, September 1999.

2. "Color and Spatial Clustering for Image Analysis with an FPGA-based Computing System," Miriam Leeser. In *Military and Aerospace Applications of Programmable Devices and Technologies Conference*, September 1998.

1. "High Level Synthesis for Designing Custom Computing Hardware," Goran Doncev, Miriam Leeser and Shantanu Tarafdar. in *IEEE Symposium on Field-Programmable Custom Computing Machines*, January 1998.

Book Chapters

10. "Digital Logic," M. Leeser and J. Brock. In T. Gonzalez, J. Diaz-Herrera, A. Tucker. Computing Handbook, Third Edition: Computer Science and Software Engineering. CRC Press, 2014.

9. "GPGPU Computing for Cloud Auditing," V. Ross and M. Leeser. In Han, K. J., Choi, B. Y., and Song, S. *High Performance Cloud Auditing and Applications*. Springer, 2014.

8. "Field Programmable Gate Arrays," Miriam Leeser. In Dr. M. Michael Vai and David R. Martinez, editors, *High Performance Embedded Computing Handbook: A Systems Perspective*. Chapman and Hall/CRC Press. pp. 217–231. June 2008.

7. "FDTD: Finite Difference Time Domain – A Case Study Using FPGAs," Wang Chen and Miriam Leeser. In Scott Hauck and Andre DeHon, editors, *Reconfigurable Computing: The Theory and Practice of FPGA-based Computation*. Morgan Kauffman. pp. 697–724, 2008.

6. "Digital Logic," Miriam Leeser. In Allen B. Tucker, Editor in Chief, *Computer Science Handbook, Second Edition*. Chapman and Hall/CRC Press. pp. 16-1 – 16-38, 2004.

5. "Implementing Filters with Programmable Logic," Miriam Leeser, Michael Bertone, Richard Chapman, and Alan Wenban. In Will Moore and Wayne Luk, eds, *More FPGAs*. Abingdon EE & CS Books, pp. 192–201, 1994.

4. "A Methodology for Reusable Hardware Proofs," Mark Aagaard and Miriam Leeser. In L. Claesen and M. Gordon, eds, *Higher Order Logic Theorem Proving and its Applications*, pp. 177–196, North-Holland, 1993.

3. "The Implementation and Proof of a Boolean Simplification System," Mark Aagaard and Miriam Leeser. In Geraint Jones and Mary Sheeran, eds, *Designing Correct Circuits, Oxford 1990*, Springer-Verlag, pp. 171–195, 1991.

2. "From Programs to Transistors: Verifying Hardware Synthesis Tools," Geoffrey Brown and Miriam Leeser. In *Hardware Specification, Verification, and Synthesis: Mathematical Aspects* Springer-Verlag Lecture Notes in Computer Science No 408, pp. 129–151, January 1990.

1. "Formally Verified Synthesis of Combinational CMOS Circuits," David Basin, Geoffrey Brown, and Miriam Leeser. In Luc Claesen, ed., *Formal VLSI Specification and Synthesis*, North-Holland, pp. 197–206, January 1990.

Invited Talks

67. *Practical, Secure Function Evaluation at Scale*, Computational Research In Boston Seminar, October 2017. Joint talk with Stratis Ioannidis.

66. *Accelerating Privacy Preserving Computations with FPGAs in the Datacenter*, Trinity College Dublin, May 2017. Also given at Xilinx Research, Dublin May 2017.

65. *Accelerating Privacy-Preserving Computations with FPGAs*, MIT Lincoln Laboratory, October 2016.

64. *Heterogeneous Computing and Software Defined Radio: Past, Present and Future, A Personal Story*, iMinds, Ghent, Belgium. August 2016.

63. *FPGAs in Software Defined Radio: Past, Present and Future*, WIreless Innovation Forum (WinnComm), March 2016.

62. *Heterogeneous computing components (ARM, FPGA, GPU, ...) for 5G wireless and beyond*, Mathworks Research Faculty Summit, June 2015.

61. *A Personal History of Reconfigurable Hardware and Software Defined Radios*, New England Workshop on Software Defined Radio (NEWSDR), May 2015.

60. *Floating Point Computations in the Multicore and Manycore Era*, Lawrence Livermore Laboratory, February 2014.

59. *Mobile wireless devices, embedded GPUs and security*, Cyber Security Professionals Meeting, Northeastern University, February 2014.

58. *Graphical Processing Units on Android Platforms & TeSCASE Testbed for Side-Channel Analysis and Security Evaluation*, at Air Force Research Lab, Rome NY. November 2013.

57. *The Mathwork Northeastern Partnership*, at Mathworks Research Faculty Summit, June 2013.

56. *Numerical Stability and Multi Core, Many Core, and GPUs, or Why are My Answers Always Different?* Energy Efficient High Performance Computing Workshop at MIT. February, 2012.

55. *Tasks and Conduits Framework for Portable Heterogeneous Architecture Applications.* GPU@BU. November 2011.

54. *How do you know your GPU or Manycore program is Correct?* Northeastern University Workshop on Advances in GPU Computing. October 2011.

53. *How do I know my GPU or multicore program is correct?* Fifteenth Annual Workshop on High-Performance Embedded Computing (HPEC2011). September 2011.

52. *How do I know my GPU or multicore floating point computations are correct?* Cambridge University Computer Laboratory, Cambridge, UK. June 2011.

51. *The Challenges of Writing Portable, Correct and High Performance Libraries for GPUs or How to Avoid the Heroics of GPU Programming.* Keynote, International Workshop on Highly-Efficient Accelerators and Reconfigurable Technologies. London, UK. June 2011.

50. *The Challenges of Writing Portable, Correct and High Performance Libraries for GPUs or How to Avoid the Heroics of GPU Programming.* Mathworks, Natick MA. April 2011.

49. *The Challenges of Writing Portable, Correct and High Performance Libraries for GPUs or How to Avoid the Heroics of GPU Programming.* Oxford University and Imperial College, London. March 2011.

48. *Floating Point Vector Processing on an FPGA*. At the Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing Workshop at Design, Automation and Test, Europe, Grenoble France. March 2011.

47. *The Challenges of Writing Portable, Correct and High Performance Libraries for GPUs or How to Avoid the Heroics of GPU Programming.* At the Institute for Mathematics and its Applications (IMA) Workshop on High Performance Computing and Emerging Architectures, Minneapolis, MN, January 2011.

46. *GPU programming and correctness in Biomedical Applications.* Distinguished Lecture Series for the Center of Parallel Computing at the University of Utah, October 2010.

45. *GPU programming: Bugs, pitfalls and the importance of correctness in biomedical and scientific applications.* Workshop on Exploiting Concurrency Efficiently and Correctly, Edinburgh Scotland. July 2010. Also given at Microsoft Research, Cambridge England. July 2010.

44. *Efficient Template Matching with Variable SizeTemplates in CUDA*. The Mathworks, Natick MA. April 2010.

43. *Accelerating Lung Tumor Tracking with Nvidia GPUs: a Case Study for GPU Library Construction.* At Workshop on GPU Computing for Biomedical Research, Harvard Medical School, Boston, MA. October 2009.

42. *Vforce: Aiding the Productivity and Portability in Reconfigurable Supercomputer Applications via Runtime Hardware Binding.* Computational Research in Boston (CRIB), March 2009. Also given at MIT Lincoln Laboratories, March 2009.

41. *Leesers Lessons or How to Get Performance Out of Your FPGA Designs and How NOT To.* Military and Aerospace Programmable Logic Devices (MAPLD) Conference. September 2008.

40. *Programming Matrix Matrix Multiply on the Playstation 3.* Air Force Research Laboratory, Rome NY. August 2008.

39. *VForce: Aiding the Productivity and Portability in Reconfigurable Supercomputer Applications via Runtime Hardware Binding.* Graduate Seminar, Electrical and Computer Engineering Department, Worcester Polytechnic Institute. March 2008.

38. *Managing Memory Hierarchies for Cacheless Architectures.* Computer Science Department Colloquium, Tufts University. February 2006. Also given to Distributed Systems Seminar, Cornell University March 2006.

37. *Adapting Parallel Backprojection to an FPGA Enhanced Distributed Computing Environment.* Workshop on Reconfigurable High Performance Computing, Air Force Research Laboratory, Rome, NY. December 2005.

36. *Reconfigurable Hardware: Overview, Applications and Future Trends.* Olin College. November 2004.

35. *Vector Signal and Image Processing Library: An FPGA Perspective.* High Performance Embedded Computing Software Initiative Meeting. MIT Lincoln Laboratories, Lexington MA. November 2003.

34. *Field Programmable Gate Arrays Accelerate Computationally Intensive and Data Intensive Applications.* Air Force Research Laboratory, Rome NY. October 2003.

33. *K-means Clustering: A Case Study in Applying Reconfigurable Hardware to Data Intensive Applications.* IEEE New Zealand North, Auckland NZ. June 2003.

32. *Reconfigurable Hardware For Data Intensive Applications: Current Successes and Future Challenges.* Electrical & Electronic Engineering Seminar, Auckland, NZ. May 2003.

31. *A Library of Parameterized Hardware Modules for Floating Point Arithmetic and Its Use.* Embedded Systems Research Group, Auckland, NZ. March 2003.

30. *Reconfigurable Hardware and Its Application to Biomedical Image Processing* Bioengineering Institute, Auckland, NZ. March 2003.

29. *Reconfigurable Hardware for Image and Signal Processing Applications: Designs and Tools.* Mathworks Corporation. June 2002.

28. *Reconfigurable Hardware for Image and Signal Processing Applications.* Northeastern University CDSP Workshop. May 2002.

27. *Parameterized Floating Point Modules and How to Use Them*, MIT Lincoln Laboratory, December 2001. Also given at Synopsys Corporation, February 2002.

26. *Hyperspectral Image Processing in Hardware.* Boston Area CenSSIS Seminar Series. Northeastern University, February 2001.

25. *Rapid Feature Identification in Satellite Imagery with Reconfigurable Hardware.* Dept. of EECS Seminar, Tufts University, February 2001.

24. *Applying Reconfigurable Hardware to Segmentation for Multispectral Imagery.* Workshop on Hyperspectral Imaging and Processing, Research and Industrial Collaboration Conference, Center for Subsurface Sensing and Imaging Systems, November 2000.

23. *Research on Rapid Prototyping and Image Processing.* Sanders, a Lockheed Martin Company, March 1999.

22. *Image Clustering on a Custom Computing Machine.* Los Alamos National Laboratory, November 1998.

21. *Using Behavioral Synthesis to Generate FPGA-based Designs.* Synopsys, Inc. Mountain View CA, November 1998.

20. *Rothko: A Three Dimensional FPGA with Applications to Image Processing.* Princeton University Department of Electrical Engineering, September 1997. (Also given at NEC Research Institute, Princeton NJ, September 1997.)

19. *HML: A Novel Hardware Description Language and its Translation to VHDL.* Brown University, February 1997. Also given at Synopsys, Inc. Mountain View CA, September 1996.

18. *High Level Synthesis Tutorial* IBM, Endicott NY, September 1995.

17. *Floating Point Division and Square Root: Algorithms and Implementations.* Northeastern University, March 1995. (Also given at Tufts University, March 1995 and University of Texas at Austin, April 1995.)

16. *Describing and Reasoning About Non-restoring Square Root with HML.* Cambridge University Computer Laboratory, July 1994.

15. *HML: A Hardware Description Language Based on Standard ML.* Oxford University Programming Research Group, July 1994.

14. *Subtractive Non-restoring Square Root: A Case Study in Verification by Principled Optimization.* Oxford University Programming Research Group, July 1994.

13. *Modeling Processors Abstractly.* Digital Equipment Corporation, Hudson, MA. January, 1994.

12. *How Formal Methods Can Help Hardware Designers.* Cornell University School of Electrical Engineering, March 1994. (Also given at CASE Center, Syracuse University. November, 1993.)

11. *Using Nuprl for Hardware Verification.* Higher Order Logic Theorem Proving Workshop, Vancouver, Canada. August, 1993.

10. *A Framework for Specifying and Designing Pipelines.* IBM T. J. Watson Research Center, Yorktown Heights, NY. July, 1993.

9. *Verification of Floating Point Hardware (and Software).* NASA Langley Research Center. Langley, VA. August, 1992.

8. *How Formal Methods Can Help Hardware Designers.* Digital Equipment Corporation, Hudson, MA. January, 1992.

7. *Using Nuprl for Hardware Verification and Synthesis.* Royal Society, London England. October 1991. (Also given at Hewlett Packard Research Laboratories, Bristol England, October 1991.)

6. *On the Interaction Between Verification and Synthesis of Digital Designs.* Princeton University Department of Electrical Engineering. September 1990. (Also given at Odyssey Research Associates, Ithaca NY, November 1990 and Syracuse University Department of Electrical and Computer Engineering, January 1991.)

5. *High Level Synthesis for Field Programmable Gate Arrays.* Xilinx Corporation, San Jose, CA. July 1990.

4. *Proven Boolean Simplification.* Synopsis, Inc. Mountain View, CA. July 1990.

3. *On the Interaction Between Verification and Synthesis of Digital Designs.* Mitsubishi Electronics, Sunnyvale CA. July 1990.

2. *From Programs to Transistors: Verifying Hardware Synthesis Tools.* NASA Goddard Space Flight Center. August 1989.

1. *A Formal Approach to the Synthesis of Combinational CMOS Circuits.* University of Toronto, Electrical Engineering Computer Group. March 1989.

Research Grants and Contracts

1. *SaTC:Massively Scalable Secure Computation Infrastructure Using FPGAs.* **National Science Foundation**, with Stratis Ioannidis. 09/01/2017 - 08/30/2017. $500,000.

2. *Optimized Virtualized Extensible Real-time Technology Utilization for RF Elements (Overture)* Subcontract from BAE Systems as part of DARPA CONverged Collaborative Elements for RF Task Operations (CONCERTO) program. $487,788.

   Hardware/Software Implementations of WiFi and LTE Communications. Mathworks. 9/2016–8/2019. $200,000.

   Privacy Preserving Data Mining over FPGAs in the Datacenter. Google Faculty Research Award, (with Stratis Ioannidis). 5/2016 – 8/2017. $67,100.

   Accelerate K-Means clustering on FPGAs in the Datacenter. Microsoft. 10/2015 – 9/2017. $55,000.

   MRI: Development of a Testbed for Side Channel Analysis and Security Evaluation (TeSCASE). **National Science Foundation.** 10/01/2013 - 09/30/2017. $500,000. With Y. Fei and D. Kaeli.

   Modeling Manycore Architectures for Easy Mapping and Acceleration of MATLAB and Simulink Applications. **Mathworks, Inc.** 9/1/2011 – 8/31/2017. $280,000.

Ensuring Reliability and Portability of Scientific Software for Heterogeneous Architectures. **National Science Foundation.** 08/01/2012 - 07/31/2016. $499,857. REU supplement. 2013. $8000.

System Modelling and Radio Technology (SMART) Laboratory. $700,000. **Mathworks, Inc.** 1/1/2012 – 12/31/2016.

A subthreshold FPGA. **MIT Lincoln Laboratory.** 09/01/2012 – 4/30/2013. $90,722.

Applying OpenCPI to FPGA and GPU Designs. **Air Force Research Laboratory** subcontract from Mercury Federal Systems. 1/1/2011 – 12/31/2011. $50,000.

A Biomedical Imaging Acceleration Testbed. **National Science Foundation** (Principal Scientist.) 12/15/2009-11/30/2012. $1,300,000. (My portion: $225,000.)

Modeling Architectures and Algorithms in Simulink. **The Mathworks, Inc.** 5/1/2007 – 8/31/2011. $240,000.

MIT Lincoln Laboratory **Scholarship for Scott Bailie**. 1/1/2010–4/30/2010. $31,568.

Accelerating Explicit State Model Checking with Reconfigurable Hardware. **Intel Corporation.** 10/1/2006 – 9/30/2010. $160,000.

A Toolkit for Implementing Image Processing Algorithms in Reconfigurable Hardware. **NSF ERC: Center for Subsurface Sensing and Imaging Systems** 9/1/2003–8/31/2010. $360,000.

API To Incorporate FPGA designs in VSIPL++ Programs. **ITT Industries.** 1/1/2005 – 5/31/2007. $135,000.

Embedded Systems for Feedback Control in Fluid Flow Applications with Gilead Tadmor. **NSF CCR Embedded and Hybrid Systems Program.** 10/15/04 –9/30/08. $300,000.

Mapping Backprojection to the Heterogeneous HPC Cluster for SAR Image Formation with Eric Miller. **DOD High Performance Computer Modernization Program.** 6/1/2004 - 5/30/3005. $110,574.

Implementation of Backprojection and other Applications on Reconfigurable Hardware. **Mercury Computer Systems, Inc.** 9/1/2003 – 8/31/2006. $187,500.

FPGA Implementation of EM Clustering. **Neural Arts, Inc.** 1/04 – 5/04. $12,123.

Embedded Systems for Feedback Mixing Control in Fluid Flow with Gilead Tadmor. **NSF CCR Embedded and Hybrid Systems Program.** 6/01/02 –5/31/05. $160,000.

A Toolkit for Implementing Image Processing Algorithms in Reconfigurable Hardware **NSF ERC: Center for Subsurface Sensing and Imaging Systems** 9/1/2001–8/31/2003. $145,000.

Image Processing Techniques for Satellite Data using Reconfigurable Technology, Graduate Student Research Program for Heather Quinn, **NASA**. 9/15/2001-9/14/2004. $70,000.

Implementation of Back Projection on Reconfigurable Hardware with Eric Miller. **Mercury Computer Systems, Inc.** 9/1/2000 – 8/31/2003. $175,000.

Analysis and Implementation of CDMA2000 Mobile Rake Receiver on Improv Systems Jazz Programmable Architecture with Masoud Salehi. **Improv Systems, Inc.**, 9/15/2000 – 9/14/2001. $50,000.

Acceleration of Scene Classification and Spectral Unmixing with Reconfigurable Computing Subcontract from **Los Alamos National Laboratory**, 9/1/1999 – 8/31/2002. $290,000.

Research Experience for Undergraduates, **National Science Foundation** 1994-1995. $5000.

Joint Research in Hardware Synthesis and Verification, **National Science Foundation**. (PI Geoffrey Brown, Co-PI Miriam Leeser. Joint research with Oxford University Programming Research Group) July, 1993 – June 1995. $20,000.

Digital Equipment Corporation Fellowship for Mark Aagaard with matching funds from National Science Foundation NYI Award. September, 1993 – August 1994. $34,000.

Toolkit Development for the Design of Floating Point Arithmetic Hardware and Software, **National Young Investigator Award, National Science Foundation**. September, 1992 – August 1998. $500,000 including matching funds.

Verification and its Applications to Automated Hardware Synthesis, **National Science Foundation**. Jan 1992 – Dec 1993. $80,000.

Digital Equipment Corporation Fellowship for Mark Aagaard. September, 1991 – August 1993. $60,000.

MTV: A Multiple Event Timing Verifier, **National Science Foundation Research Initiation Award**. July, 1991 – June, 1993. $60,000.

Hardware Specification, Verification and Synthesis: Mathematical Aspects. Workshop sponsored by **Army Research Office** through Mathematical Sciences Institute. July, 1989. $15,000.

External Educational and Equipment Grants

Xilinx Corporation Zynq board. $2495. 2013.

Altera Corporation DE1 boards. $3750. 2013.

NVIDIA teaching center. Northeastern received $20,000 in hardware donations. 2012.

Xilinx field programmable hardware and software. 2012. $7989.

Xilinx field programmable hardware and software. 2006-2008. $5,682.

Mercury Computers FPGA system and software. 2004-2005. $117,600.

Xilinx field programmable hardware and software. 2002-2005. $268,590.

Altera field programmable hardware, 1999. $14,730.

Xilinx field programmable hardware and software. 1998-9. $291,969.

Wind River Systems Tornado Development System. 1998. $16,500.

Synplicity Development System, 1998. $480,000.

Altera field programmable hardware and software. January – June 1996. $44,000.

Xilinx field programmable hardware and software. June 1994–June 1996. $200,160.

Hewlett Packard University Equipment Grant: HP Logic Analyzer, 1994. $30,575.

MOSIS fabrication of EE 539 VLSI chips, supported by the National Science Foundation. 1993–95. $23,100.

Xilinx Mentor Extension Package, 1993. $11,995.

Tektronix workstations, 1993. $4,500.

Hewlett-Packard workstations, 1993. $16,000.

FPGA Design Software. Altera Corporation, 1992. $14,000.

FPGA Design Software and Hardware. Xilinx Corporation, 1990. $5,000.

Internal Grants (Northeastern University)

Tier 1: "Development of an Adaptive Clinician-Friendly Virtual Rehabilitation System and its Evaluation in Post-Operative Shoulder Therapy." With Dagmar Sternad and Aimee Seitz. 2013-2014 $50000.

Research Students Supervised
PhD Degrees Supervised

18. Chao Liu, "Unified Tasks and Conduits for Programming on Heterogeneous Computing Platforms." Northeastern University, December, 2017.

17. Xin Fang, "Privacy Preserving Computations Accelerated using FPGA Overlays." Northeastern University, August 2017.

16. Benjamin Drozdenko, "Enabling Protocol Coexistence: Hardware-Software Codesign of Wireless Transceivers on Heterogeneous Computing Architectures." Northeastern University, May 2017. Assistant Profesor at Louisiana Tech.

15. Peter Grossmann, "Design and Analysis of Minimum Energy FPGAs." Northeastern University, May 2013. Currently at MIT Lincoln Laboratory.

14. James Brock, "An Environment to Support GPU and Multicore Programming for Rapid, High Performance, Application Deployment." Northeastern University, August 2012. Currently at Mathworks.

13. Nicholas Moore, "Kernel Specialization for Improved Adaptability and Performance on Graphics Processing Units (GPUs)." Northeastern University, June 2012. Currently at Mathworks.

12. Abderrahmane Bennis, "Implementing a Highly Parameterized Digital PIV System On Reconfigurable Hardware." Northeastern University, August 2010. Currently at IBM.

11. Xiaojun Wang, "Variable Precision Floating-Point Divide and Square Root for Efficient FPGA Implementation of Image and Signal Processing Algorithms." Northeastern University, January 2008. Currently at Airvana.

10. Wang Chen, "Acceleration of the 3D FDTD Algorithm in Fixed-point Arithmetic using Reconfigurable Hardware." Northeastern University, August 2007. Currently at Mathworks, Inc.

9. Haiqian Yu, "Optimizing Data Intensive Window-based Image Processing on Reconfigurable Hardware Boards." Northeastern University, January 2007. Currently at Teradyne, Inc.

8. Heather Quinn, "Runtime Tools for Hardware/Software Systems with Reconfigurable Hardware." Northeastern University, August 2004. Currently at Los Alamos National Laboratory.

7. Juan Carlos Rojas, "Multimedia Macros for Portable Optimized Programs." Northeastern University, August 2003.

6. Silviu Chiricescu, "Parametric Analysis of a Dynamically Reconfigurable Three-Dimensional FPGA.", Northeastern University, June 2000.

5. Valerie Ohm, "Power Estimation for Combinational and Sequential CMOS Circuits using Graph-Based Methods." Cornell University, May 1999.

4. Shantanu Tarafdar, "A Data-Transfer Model for High Level Synthesis and Its Application in Storage and Interconnect Optimization." Cornell University, May 1998. Currently Member, Technical Staff, Synopsys.

3. Peter Soderquist, "Cache-Sensitive Architectural Optimizations for MPEG-2 Video Decoding." Cornell University, May 1998. Currently at Apple Computers.

2. Mark Linderman, "Simulation of Digital Circuits in the Presence of Uncertainty." Cornell University, January 1995. Currently Principal Researcher, Air Force Research Laboratory Information Directorate.

1. Mark Aagaard, "A Framework for the Specification, Design, and Verification of Pipelines with Structural Hazards." Cornell University, January 1995. Currently Associate Professor, University of Waterloo Dept of Electrical and Computer Engineering.

MS Theses Supervised

30. Kai Huang, "K-means Parallelism on FPGA," Northeastern University, December 2017.

29. Majid Sabbagh, "Accelerating Cardiac MRI Compressed Sensing Image Reconstruction using Graphics Processing Units," Northeastern University, April 2016.

28. Mahsa Bayati, "Parallel Methods for Protein Coordinate Conversion," Northeastern University, May 2015.

27. Jonathon Pendlum, "CRASH: Cognitive Radio Accelerated with Software and Hardware," Northeastern University, April 2014.

26. Xin Fang, "Variable Precision Floating Point Reciprocal, Divider and Square Root for Major FPGA Vendors," Northeastern University, July 2013.

25. David Kusinsky, "FPGA-based Hyperspectral Covariance Coprocessor for Size, Weight, and Power Constrained Platforms." Northeastern University, April 2013.

24. George Eichinger, "CRUSH: Cognitive Radio Universal Software Hardware," Northeastern University, April 2012.

23. Mary Ellen Tie, "Accelerating Explicit State Model Checking on an FPGA: PHAST," Northeastern University, February 2012.

22. Devon Yablonski, "Numerical Accuracy Differences in CPU and GPGPU Codes," Northeastern University, August 2011. Currently at Mercury Computer Systems.

21. Jainik Kathiara, "The Unified Floating Point Vector Co-processor for Reconfigurable Hardware," Northeastern University, January 2011. Currently at Analog Devices.

20. Scott Bailie, "An FPGA Implementation of Incremental Clustering for Radar Pulse Deinterleaving," Northeastern University, May 2010. Currently at MIT Lincoln Laboratory.

19. Sherman Braganza, "Phase Unwrapping on Reconfigurable Hardware and Graphics Processors." Northeastern University, August 2008. Currently at Matworks, Inc.

18. Benjamin Cordes, "Parallel Backprojection: A Case Study in High Performance Reconfigurable Computing." Northeastern University, May 2008. Continued to PhD.

17. Nicholas Moore, "Vforce: VSIPL++ for Reconfigurable Computing Environments." Northeastern University, defended December 2007. Degree awarded 2011. Continued on to PhD.

16. Albert A. Conti III, "A Hardware/Software System for Adaptive Beamforming." Northeastern University, January 2007. Currently at Mitre Coproration.

15. Joshua Noseworthy, "Enabling Communications Between an FPGA's Embedded Processor and its Reconfigurable Resources." Northeastern University, August 2005. Currently at Mercury Computers, Inc.

14. Shawn Miller, "Enabling a Real-time Solution to Retinal Vascular Tracing Using FPGAs." Northeastern University, April 2004. Currently at Mitre Corporation.

13. Wang Chen, "An FPGA Implementation of the 2D FDTD Algorithm." Northeastern University, August 2003. Continued on to PhD.

12. Haiqian Yu, "Memory Architecture of Data Intensive Image Processing Algorithms in Reconfigurable Hardware." Northeastern University, August 2003. Continued on to PhD.

11. Michael Estlick, "An FPGA Implementation of the K-Means Algorithm for Image Processing." Northeastern University, September 2002. Currently at AMD.

10. Srdjan Coric, "Parallel-Beam Backprojection: an FPGA Implementation Optimized for Medical Imaging." Northeastern University, September 2002.

9. Pavle Belanovic, "Library of Parameterized Modules for Floating-Point Arithmetic with an Example Application." Northeastern University, June 2002. Continued on to PhD at University of Vienna.

8. Natalya Kitaryeva, "K-Means Clustering for Color Image Processing on a Reconfigurable Hardware Board." Northeastern University, June 2001. First employed at Trebia, Inc.

7. Heather Quinn, "Image Processing Designs in JHDL, a Java-based Hardware Description Language." Northeastern University, December 2000. Continued on to PhD.

6. Ali Shankiti, "Implementing a RAKE Receiver on an FPGA-based Computer System." Northeastern University, September 1999. First employed at Motorola, Inc.

5. Zixin Yin, "Global and Incremental Floorplanning for High-Level Synthesis." Northeastern University, December 1998.

4. Goran Doncev, "Mapping DSP Systems onto FPGAs Using Behavioral Synthesis: A Case Study." Northeastern University, June 1998. First employed at Phillips Semiconductor.

3. Yanbing Li, "HML: An Innovative Hardware Description Language and Its Translation to VHDL." Cornell University, August 1995. Went on to complete PhD at Princeton University.

2. Peter Soderquist, "Area and Performance Tradeoffs in Floating-Point Division and Square Root Implementations." Cornell University, January 1995. Continued on to complete PhD.

1. Mark Aagaard, "A Formally Verified System for Logic Synthesis." Cornell University, January 1992. Continued on to complete PhD.

Current Students – Advisor, Northeastern University

Mahsa Bayati, PhD; Janki Bhimani, PhD; Mehmet Gungor, PhD; Kai Huang, PhD; Suranga Handagala, PhD; Mohamed Mohamed, MS; John Terragnoli, MS; Jieming Xu, PhD.

MS Projects Supervised

17. Matthew Zimmermann, "Implementing the IEEE 802.11a Transmitter on the Xilinx Zynq SoC." Northeastern University, December 2015.

16. Nikhil Shelke, "Optimization and Analysis of Image Processing performance by porting Integral Image Calculation on parallel processing techniques." Northeastern University, December, 2014.

15. Shardul Sathe, "Optimization of Image Registration method using OpenMP as parallel processing technique." Northeastern University, December 2014.

14. Max Beckett, "Tasks and Conduits: A Task and Data Parallel Framework for GPU Computing." Northeastern University, April 2013.

13. Shailesh Patel, "Implementation and Synthesis of 3x3 QR Decomposition using Verilog." Northeastern University, July 2007.

12. Hai Nguyen, "Specifying and Synthesizing an Ethernet Media Access Controller Receiver at the Behavioral Level with SystemC." Northeastern University, September 2002.

11. Tao He, "A Low-Frequency All-Digital Phase-Locked Loop implementation in an FPGA." Northeastern University, March 2001.

10. Chih-Chieh Huang, "Implementing Color Histogramming in Reconfigurable Hardware." Northeastern University, August 2000.

9. Todor Mitictchev, "Translation from Image Operators to Efficient Pixel Implementations in Java." Northeastern University, September 1999.

8. Karen Matulis, "Implementing and Designing a Speed Feedback Module on an FPGA-based System." Northeastern University, December 1998.

7. Valerie Ohm, "Generating MOSIS Chips with the Alliance Toolkit."Cornell University, May 1994.

6. M. Bertone, "Implementing Arithmetic Hardware with FPGAs."Cornell University, May 1994.

5. J. deGroot, "Implementing Arithmetic Hardware with FPGAs." Cornell University, May 1994.

4. E. Leung, "A VHDL Implementation of the Number Game." Cornell University, May 1994.

3. M. Ghosh, "Support for FPGAs in the BEDROC System." Cornell University, May 1993.

2. D. Cooper, "Hardware Pascal: A high-level language interface to BEDROC." Cornell University, May 1991.

1. M. Dennison, "Proving a Multiplier Correct." Cornell University, May 1989.

Thesis Committee Member – Northeastern University

Ramanathan Subramanian, PhD. "Link layer Designs for Short-range Wireless Access Spanning ISM to mmWave Bands." April 2017.
Meghan Huber, PhD in Bioengineering. "Assessing and Enhancing Complex Skill Learning with Virtual Environments: Basic Insights for Motor Rehabilitation." June 2016.
Rahman Doost-Mohammady, PhD. "Efficient Wireless Spectrum Access: Protocols, Analysis and Applications." December, 2014.
Hamed Tabkhi, PhD. "High-Performance Power-Efficient Solutions for Pervasive Embedded Vision Computing." August 2014.
Jiaxing Zhang, PhD. "Integrating Algorithm-Level Design and System-Level Design through

Specification Synthesis." August, 2014.
Cory Brett, MS. "Efficient Implementations of Hyperspectral Remote Sensing Algorithms." April 2014.
Juan Carlos Martinez Santos, PhD. "Architectural Support for Software Security." August 2013.
Cihan Tunc, MS. "Variation and Defect Tolerance for Nano Crossbars." April 2010.
Enqiang Sun, MS. "A Binary Instrumentation Tool for the Black Fin Processor." August 2009.
Dana Schaa, MS. "Modeling Execution and Predicting Performance in Multi-GPU Environments." August 2009.
Rajaa Alqudah, MS. "On the Effects of Multiple Beacons on Localization for Wireless Sensor Networks." July 2007.
Hossein Asadi, PhD. "Soft Error Modeling and Remediation in Digital Systems." May 2007.
Prasad Mandalapu, MS. "Verilog models for synthesizable VLSI array architectures derived from algorithmic specifications," August 2004.
Demetris Galatopoullos, EE. "JavaPorts: An Environment for Distributed Component-based processing in Heterogeneous clusters of Workstations," November 2003.
Gabriel Eirea, MS. "Hardware Implementation of a Sensorless Control Algorithm for Permanent Magnet Synchronous Motors," July 2001.
Andrew Stone, PhD. "DG2VHDL: Methods and tools for the synthesis of scalable parallel VLSI architectures from abstract algorithmic specifications," June 2001.
Jin Qian, MS. "VHDL Synthesis of A Huffman Code Generator as an ASIC," September 1999.
Ryan Tewell, MS. "Development and Execution of Real-time Three-dimensional Animations of Trident Missile Operations Using the Simulation-Based Test and Evaluation Capability," August 1998.
Shuichi Wu, PhD. "Reverse Modeling using a Neural Network Approach," July 1998.
Fraya Kaufman, MS. "An Analysis of 3-D Architectures for Field Programmable Gate Arrays," May 1998.
Juan Carlos Rojas, MS. "Chromaticity Histograms for Real-Time Object Detection," August 1997.
Dev Patel, MS. "Using a Formal Methods Approach to Study the Necessity of Including an Explicit Hardware/Software Interface Specification in a Reference Model," August 1997.
Kwok Lee, MS. "A Mobile Environment Simulation Testbed," September 1996.

Thesis Committee Member – External

Mohammad Reza Mohammadnia, PhD. "Precision and Reliability of Application Specific Designs on FPGA." Simon Fraser University, Canada, 2017.

Vipin Kizheppatt, PhD. "Design Automation for Partially Reconfigurable Adaptive Systems." National Technological University, Singapore, 2014.

Thesis Committee Member – Cornell University

David Cooper, PhD (CS), 1995. John O'Leary, PhD, 1995. Lawrence Prince, MS 1995. Adam Webber, PhD(CS) 1993. Richard Chapman, PhD(CS) 1993. Aatish Dedhia, MS 1993. Deborah Marr, MS 1992. Peter DelVecchio, MS 1990. Chee-Keng Chang, MS 1990.

Undergraduate Research Projects Supervised – Northeastern University

Tuan Dao, Spring, 2016; Spring 2017. Brian Crafton, Spring 2016. Lucas Jaffe, Fall 2014. Kevin Langer, Summer 2014. Taylor Skilling Spring 2014 – Fall 2015. Meghan Wood, Fall 2014. Paul Ozog, "UARP: Underwater Acoustic Radio Peripheral." Jan – Sept, 2009. Joseph Tarkoff, "Investigation for VSIPL++ FPGA API." Jan – June, 2005. Kris Kieltyka, "VSIPL++ Coding for FPGA API." Summer, 2005. Josh Noseworthy, "Investigation of Xilinx Design Generator for Signal Processing Applications. " 2002–2003. Seth Molloy, "Investigation of HandelC and Celoxica for Generating FPGA Designs." 2002–2003. Natalya Kitaryeva, "Design of Image Processing Components on FPGAs." 1998–1999.

Undergraduate Research Projects Supervised – Cornell

J. V. Orellana "PLD Implementation of a DTMF receiver using Altera's Hardware Description Language," Summer, 1995.
K. Sripandidkulchai, "Implementation of a DTMF Receiver in VHDL," Summer, 1995.
P. Banerjee, "Design Tools for Field Programmable Logic ," 1994–95.
P. Banerjee, "Implementing the Jeopardy Game with FPGAs," Spring 1994.
R. Casas, "A Universal Assembler," 1993–94.
Funded by GE Faculty for the Future Award.
M. Bertone, "Implementing Designs for FPGAs," 1992–93.
R. Casas, "An Assembler for Hunt's Architecture," 1992–93.
E. Leung, "Digital Design with Mentor Graphics Tools," Spring 1993.
E. Teachout, "A Generic Assembler for Multiple Computer Architectures," 1991–92.
Funded by Moore Undergraduate Research Fellowship.
J. Cavilieri, "Using Xilinx FPGA Design Tools," Spring 1991.

Professional Activities

Member ACM SIGDA Technical Committee on FPGAs and Reconfigurable Computing (TC-FPGA), 2015 –present.

FCCM Panel of Experts, 20th Anniversary of FCCM, 2012.

Conference Leadership Positions
General Chair, 20th IEEE International Conference on Application-specific Systems, Architectures and Processors, Boston MA, 2009.
Co-chair, Reconfig 2009 conference track on Reconfiguration Techniques.
Publications Chair, IEEE High Performance Extreme Computing (HPEC) 2012-2014.
Co-Chair, PhD forum, Field Programmable Logic (FPL) conference, 2013.
Program Chair, IEEE Symposium on Field Programmable Custom Computing Machines (FCCM), 2013. *General Chair*, IEEE Symposium on Field Programmable Custom Computing Machines (FCCM), 2014. *Steering Committee*, IEEE Symposium on Field Programmable Custom Computing Machines (FCCM), 2013-17. *General Chair*, International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies (HEART) 2015. *Steering Committee*, International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies (HEART) 2015-17. *Publicity Chair*, International Symposium on Highly-Efficient

Accelerators and Reconfigurable Technologies, 2014. *General Chair*, International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies, 2015. *General Chair*, New England Workshop on SOftware Defined Radio (NEW-SDR). June, 2016.

Workshop Organizer

Organizer, Panel "Different Architectures, Different Times: Reproducibility and Repeatability in High Performance Computing " at *Supercomputing*, 2016.
New England Workshop on Software Defined Radio (NEW-SDR), Northeastern University, May 2016.
Organizer, Birds of a Feather Sesson "Reproducibility of High Performance Codes and Simulations Tools, Techniques, Debugging" at *Supercomputing*, 2015.
New England Workshop on Software Defined Radio (NEW-SDR), Northeastern University, May 2012.
Workshop on General-Purpose Computation on Graphics Processing Units, 2007-10.
New England Symposium on Formal Hardware Verification, Boston, MA 2007.
Hardware Synthesis and Verification Workshop, Ithaca NY, 1996.
Expanding Your Horizons: Logic Circuits Workshop for 6-8th grade girls to encourage interest in careers in Computer Engineering. Ithaca NY, November 1994.
MSI Workshop on Hardware Specification, Verification, and Synthesis, July 1989.

Panelist and Funding Agency Reviews
Israel Science Foundation, 2017. *NASA Advanced Information Systems Technology*, 2014, 2017. *Department of Energy CAREER proposals*, 2012. *National Science Foundation CISE/CNS Programs*, 2005, 2009, 2012, 2014, 2015, 2017.
Future Faculty Workshop, Northeastern University 2012.
Olin College Expo, 2005 – 08. *National Science Foundation Information Technology Research*, 2000.
National Science Foundation Graduate Research Fellowship Program, 1996–1998.
National Science Foundation Undergraduate Faculty Enhancement Program, 1994.
National Science Foundation Instructional Laboratory Improvement Program, 1993.
Workshop on Women in Science and Engineering, Ithaca NY, April 1989.

Program Committee Member
Designing Correct Circuits, 1996. Design Automation and Test Europe, 2006-11.
Engineering of Reconfigurable Systems and Algorithms, 2001–2011.
Field Programmable Logic, 2006-17. FPGAs for Software Programmers, 2014, 2016-17. Formal Methods in Computer Aided Design, 1996.
Frontiers of GPU Computing, 2010-2012. Frontiers of Heterogeneous Computing, 2013.
General Purpose Processing on Graphics Processing Units, 2011.
High-Performance Reconfigurable Computing Technology and Applications, 2010. IEEE High Performance Extreme Computing, 1999–2017. IEEE Symposium on Field-Programmable Custom Computing Machines, 2006-17.
IEEE International Conference on Application-specific Systems, Architectures and Processors, 2007–2012. IEEE International Parallel & Distributed Processing Symposium, 2013-15.
IEEE Symposium on Application Specific Processors, 2011.

International Conference on Computer Design, 1994–96, 1999–2001.
International Conference on Computer-Aided Design, 1999.
International Conference on Field-Programmable Technology, 2002–2004, 2009-17.
International Conference on ReConFigurable Computing and FPGAs 2008–10.
International Conference on Theorem Provers in Circuit Design 1994.
International Symposium on Field-Programmable Gate Arrays, 2001–2003, 2006-17.
International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies, 2014-2017.
International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC), 2017.
International Workshop on High Performance Dynamic Reconfigurable Systems and Networks, 2016-17.
International Workshop on Higher Order Logic Theorem Proving, 1992, 1995.
International Workshop on Frontiers of Heterogeneous Computing, 2013.
International Workshop on Heterogeneous High-performance Reconfigurable Computing, 2015-17.
Reconfigurable Architectures Workshop 2009-17.
Symposium on Application Accelerators in HPC 2009-12.
Supercomputing Technical Poster Committee, 2015.

Reviewer
ACM/IEEE Design Automation Conference. ACM Symposium on Real-Time System Software. ACM Transactions on Computer Systems. ACM Transactions on Design Automation of Electronic Systems. ACM Transactions on Embedded Computer Systems. ACM Transactions on Programming Languages and Systems. ACM Transactions on Reconfigurable Technology. ACM Workshop on Formal Methods in VLSI Design. Department of Energy Early CAREER grants. Design Automation and Test Europe. Engineering and Physical Sciences Research Council, UK. European Design Automation Conference. European Signal Processing Conference. EURASIP Journal on Applied Signal Processing. Evolving Systems Journal, Springer. Formal Methods in System Design: An International Journal. IBM Journal of Research and Development. IEE Systems E. IEE Proceedings on Computers & Digital Techniques. IEE Proceedings on Circuits, Devices & Systems. IEEE Communications Magazine. IEEE Computer Magazine. IEEE Design and Test Magazine. IEEE Embedded Systems Letters. IEEE Journal on Emerging and Selected Topics in Circuits and Systems. IEEE Journal of Solid-State Circuits.IEEE Signal Processing Letters. IEEE Transactions on Biomedical Engineering. IEEE Transactions on Circuits and Systems. IEEE Transactions on Circuits and Systems II. IEEE Transactions on Circuits and Systems for Video Technology. IEEE Transactions on Computational Imaging. IEEE Transactions on Computers.IEEE Transactions on Computer-Aided Design. IEEE Transactions on Computing in Science and Engineering. IEEE Transactions on Education. IEEE Transactions on Knowledge and Data Engineering. IEEE Transactions on Image Processing. IEEE Transactions on Parallel and Distributed Systems. IEEE Micro. IEEE Transactions on VLSI Systems. IET Computers & Digital Techniques. IET Circuits, Devices & Systems. IET Electronics Letters. IFIP Workshop on Applied Formal Methods for Correct VLSI Design. Information Processing Letters. Innovative Parallel Computing Conference. International Conference On Computer Aided

Design. International Conference on ReConFigurable Computing and FPGAs. International Journal of Embedded Systems. International Journal of Reconfigurable Computing. International Symposium on Circuits and Systems (ISCAS). International Symposium on Code Generation and Optimization (CGO). International Symposium on Microarchitecture. International Workshop on Frontier of GPU Computing. Integration, the VLSI Journal. Israel Science Foundation. Journal of Biomedical Optics. Journal of Electrical and Computer Engineering. Journal of Parallel and Distributed Computing (Elsevier). Journal of Real-Time Image Processing. Journal of Supercomputing. Journal of Systems Architecture. Journal of VLSI Signal Processing. Journal of Signal Processing Systems. Kluwer Academic Publisher. McGraw Hill. Medical Physics. Microelectronics Journal. Microprocessors and Microsystems. National Science Foundation. Natural Sciences and Engineering Research Council of Canada. Oxford University Press. Physical Communications Journal published by Elsevier. Reconfigurable Supercomputing Summer Institute.Transactions on VLSI Signal Processing. University Video Communications. VLSI Design.

Department and University Service – Northeastern

Interim Chair, Electrical and Computer Engineering, 2016 - December, 2017.
Chair, ECE general recruiting committee. 2016.
Member, NEU ITS Five Year Strategic Planning committee. 2015 - 2016.
Member, Bio-engineering chair search committee. 2014 - 2015.
Member, STRIDE committee, Advance Grant, 2012- 2016.
Member, COE Computer System Committee 2011- 2015.
Member, COE Academic and research infrastructure committee 2015-present.
Faculty Mentor: Prof. Ningfang Mi and Prof. Gunar Schirner, 2009 -2016.
Director, Communications and Digital Signal Processing Center, 2011-2015.
Coordinator, Computer Engineering Teaching Group. 2012, 2014-15.
Chair, NEU Research Oversight Committee, 2013-14.
Member, NEU Research Oversight committee, 2012-13.
Chair, ECE Chair Search committee, 2012-13.
Member, ECE Tenure and Promotion Committee: 2012-2014, 2004–2006, 2000–2002.
Member, Physics Department Chair search committee, Spring 2012. Member, COE Tenure and Promotion Committee: 2011-12.
Co-Director, Communications and Digital Signal Processing Center, 2010-11.
Member, BioEngineering PhD Committee 2009-10.
Member, Advance Advisory Board 2008-present.
Member, IS Academic Advisory Committee, 2009-10.
Member, Senate Financial Affairs Committee, 2009-10.
Co-chair, Review Committee for Prof. Zoloth, Dean of Bouve. Spring 2009.
Member, COE College Computing Committee 2008-2009.
Member, ECE Department Hiring Committee 2008–2009.
Co-chair, ECE Department Hiring Committee 2007–2008.
Member, College of Engineering Dean Search Committee 2006–07.
Member, Committee to evaluate Prof. Furth, Spring 2007.
Member, ECE Department Undergraduate Study Committee, Fall 2003 – Spring 2007.
Faculty Mentor: Prof. Jennifer Dy and Prof. Xinping Zhu.

Member, ECE Department Hiring Committee 2005– 2006.
Chair, ECE Department Hiring Committee, Fall 2004 – Spring 2005.
Member Northeastern University Benefits Study Committee, Sept 2000 – Spring 2006.
Member, ECE Department Interim Chair Search Committee, Spring 2004.
Member, ECE Dept Undergraduate Study Committee, Fall 2001 – Spring 2002
Member, Review Committee for Prof. Finkelstein, Dean of Computer Science. Spring 2002
Member, ECE Department Faculty Evaluation Committee Winter 2002.
Member, English Department Chair Search Committee, Spring 2001.
Member ECE Dept Education Committee, Sept 1999–June 2000.
Member COE Dean's Faculty Council, Sept 1999 – June 2000.
Member Northeastern University Faculty Senate Financial Affairs Committee, September 1998 – June 2000. Member Northeastern University Five Year Financial Planning Committee, March 1999 – 2000.
Member Northeastern University Funding Priorities Committee, September 1998 – 1999.
Member ECE Dept Computer Engineering Curriculum committee, Sept 1998 – Sept 1999